SHARP SERVICE MANUAL

CODE: 00ZAR5132TM1E

DIGITAL COPIER NO.2

MODEL AR-5132

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Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

CAUTION

This copier machine is a class 1 laser product that complies with 21CFR 1040.10 and 1040.11 of the CDRH standard and IEC825. This means that this machine does not produce hazardous laser radiation. The use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

This laser radiation is not a danger to the skin, but when an exact focusing of the laser beam is achieved on the eye's retina, there is the danger of spot damage to the retina.

The following cautions must be observed to avoid exposure of the laser beam to your eyes at the time of servicing.

1) When a problem in the laser optical unit has occurred, the whole optical unit must be exchanged as a unit, not as individual parts.
2) Do not look into the machine with the main switch turned on after removing the developer unit, toner cartridge, and drum cartridge.
3) Do not look into the laser beam exposure slit of the laser optical unit with the connector connected when removing and installing the optical system.
4) The safety interlock switch is equipped.

   Do not defeat the safety interlock by inserting wedges or other items into the switch slot.

CLASS 1
LASER PRODUCT

LASER KLASSE 1

LASER WAVE – LENGTH : 785 ± 15nm
Pulse times :
Out put power : 0.3mW ~ 0.6mW

CAUTION

INVISIBLE LASER RADIATION,
WHEN OPEN AND INTERLOCKS DEFEATED.
AVOID EXPOSURE TO BEAM.

VORSICHT

UNSICHTBARE LASERSTRAHLUNG,
WENN ABDECKUNG GEÖFFNET UND
SICHERHEITSVERRIEGELUNG ÜBERBRÜCKT.
NICHT DEM STRAHL AUSSETZEN.

VARO !

AVATTAESSA JA SUOJALUKITUS
OHITETTAESSA OLET ALTTIINA
NÄKYMÄTTÖMÄLLE LASERSÄTEILYLLE ÄLÄ
KATSO SÄTEESEEN.

ADVARSEL

USYNLIG LASERSTRÅLNING VED ÅBNING, NÅR
SIKKERHEDSBRYDERE ER UDE AF
FUNKTION. UNDGÅ UDSAETTELSE FOR
STRÅLNING.

VARNING !

OSYNLIG LASERSTRÅLNING NÄR DENNA DEL
ÄR ÖPPNAD OCH SPÄRREN ÄR URKOPPLAD.
BETRAKTA EJ STRÅLEN. – STRÅLEN ÄR
FARLIG.

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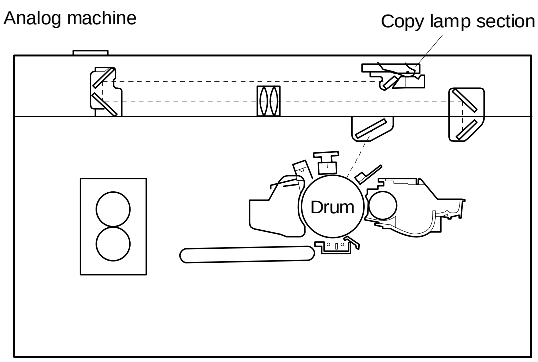
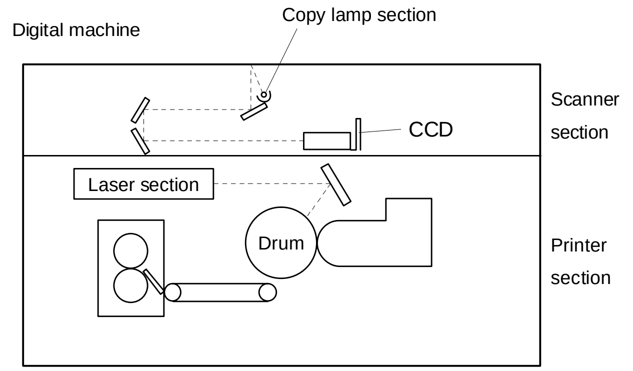
[1] PRINCIPLES OF THE DIGITAL COPIER

1. Difference in structure from analog copiers

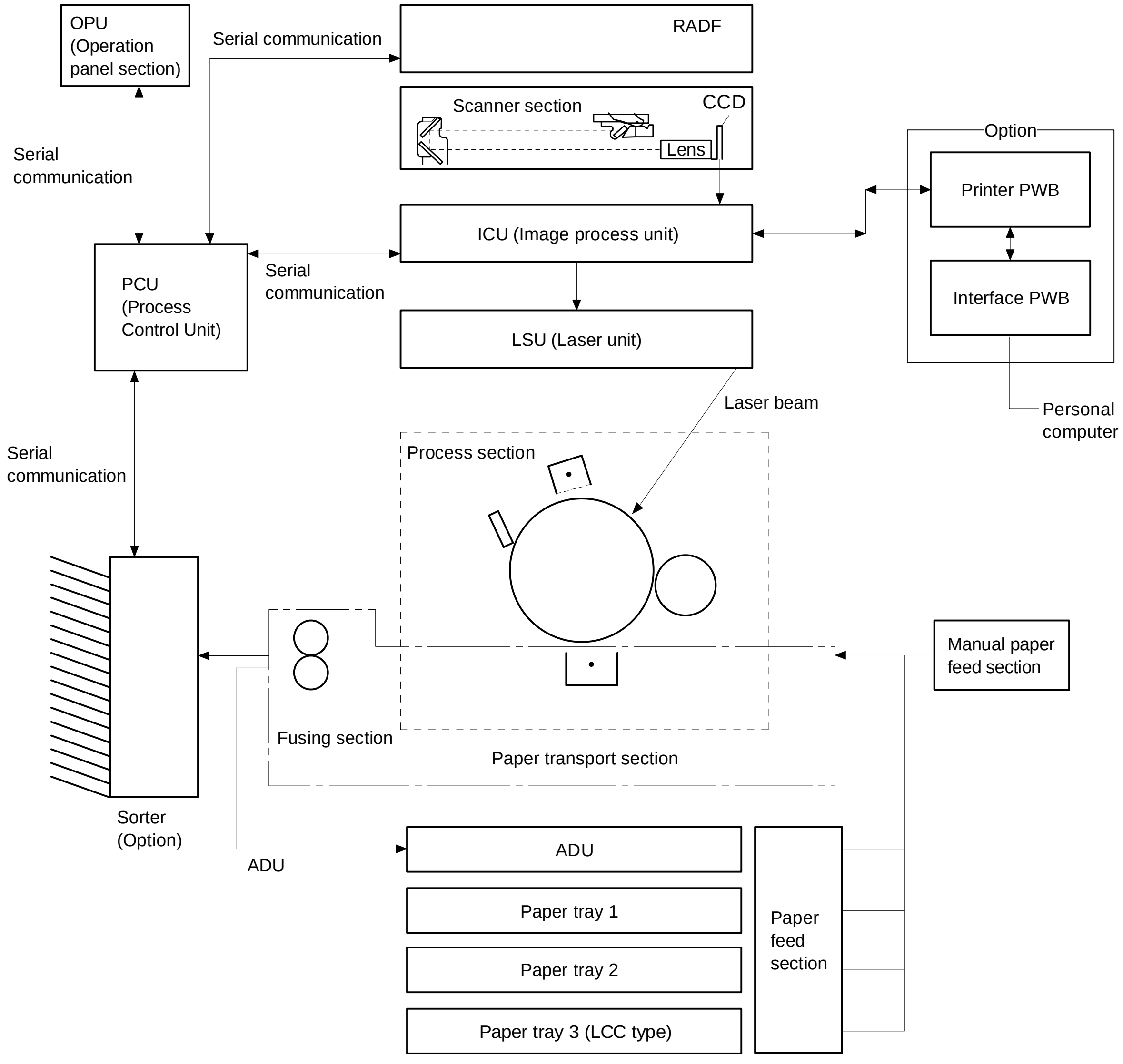




The digital copier is composed of the scanner section and the printer section. (Refer to the figures.)

In the digital copier, the reflected light is not directly radiated onto the OPC drum as in the analog copiers.

2. Basic composition of the digital copier



(1) Basic operations of copying

① Image data are scanned in the scanner section and sent to the image process (ICU) PWB.

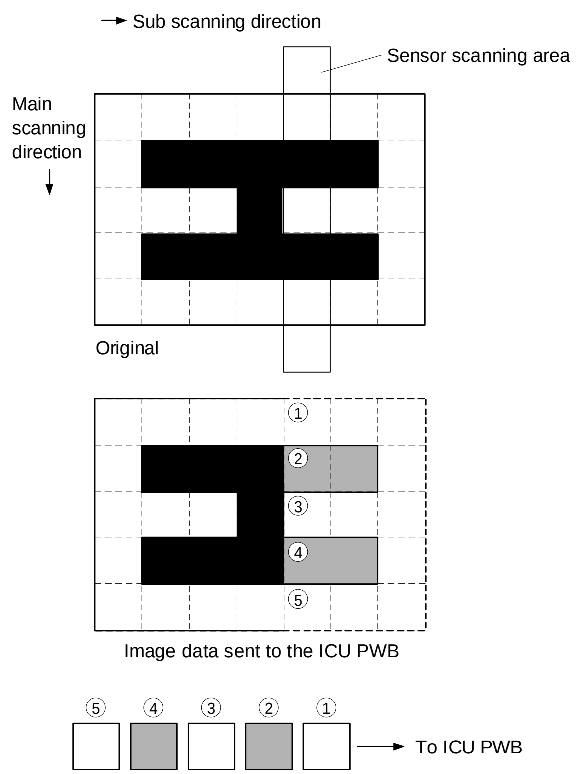
② The data are converted into printable data in the circuit of the image process (ICU) PWB.

③ The data are printed in the printer section.

3. Scanner section

(1) How to scan an document

The scanner is provided with sensors which are arranged on one line. These sensors scan a horizontal line of an document at a time and the data are outputted sequentially. After completion of the line, the next line is scanned. The operation is repeated until one page is completed. The figure below shows that the images scanned by the sensors are sent to the ICU PWB sequentially.



The direction of the lines is called the "main scanning direction" and the direction of scanning the "sub scanning direction."

The above figure shows four elements in one line. Actually, however, there are thousands of elements in one line. The light receiving elements called CCD are used.

The resolution is an index value to express the capacity of scanners. The resolution shows how many light receiving elements are used in one inch (dpi, dot per inch).

While the sub scanning direction is used to control the motor which drives the optical system and to adjust the resolution to take in the images.

(2) Basic structure of the scanner section

The scanner unit is the scanning section of the digital optical system. The light from the halogen lamp (which is driven by the DC power to suppress ripples) is reflected by the document and passed through three mirrors and the reduction lens to form images on the CCD elements (image sensors). This system is called the reduction type image sensor system. The light image (photo energy) formed on the CCD elements are converted into electrical signals (analog signals) by the CCD elements (Photo conversion).The output signals (analog signals) are converted into digital signals (A/D conversion) to perform various image processes. The resolution at that time is 400dpi.

4. Laser unit

The image data sent from the ICU (image process PWB) are passed to the LSU (laser unit) and converted into laser beams.

(1) Basic structure

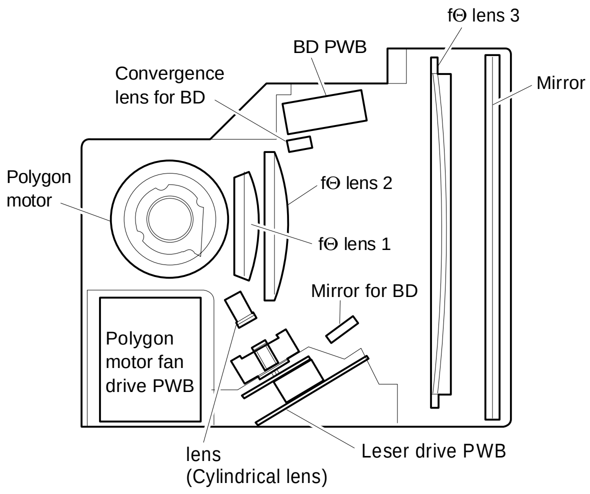
The LSU unit is the writing section of the digital optical system. The semiconductor laser is used as the light source. Images are formed by the polygon mirror and the fθ lens on the OPC drum.

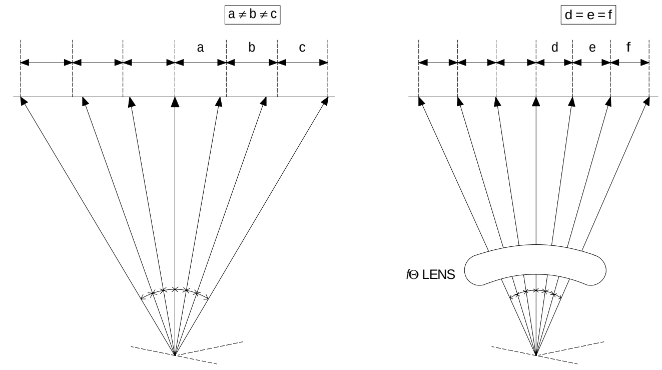
The internal structure is shown in the figure on the next page. The image data from the ICU are converted into DUTY signals for every gradations (256 steps), and the semiconductor laser on the laser emitting PWB is turned on/off according to the DUTY. The laser beams are passed through the collimator lens, the slit, the cylindrical lens, the polygon mirror, the fθ lens, and the mirror to form images in the shaft direction (main scanning direction) of the OPC drum. The laser emitting PWB is provided with the APC (Auto Power Control) to eliminate fluctuations in the laser power. The BD PWB serves to measure the writing point for the laser.

(2) Composition

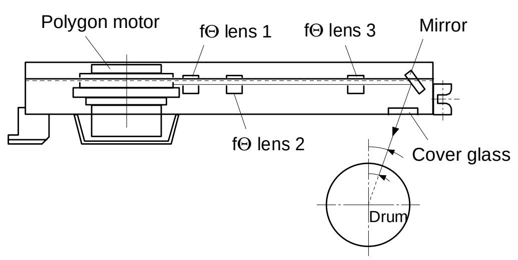
Effective scanning width:	302 mm
Resolution:	400 dpi
Beam diameter:	main scanning 75 µm, sub scanning 90 µm
Image surface power:	0.3mW ~ 0.6mW
Polygon motor:	Brushless DC motor
	No. of mirrors → 6

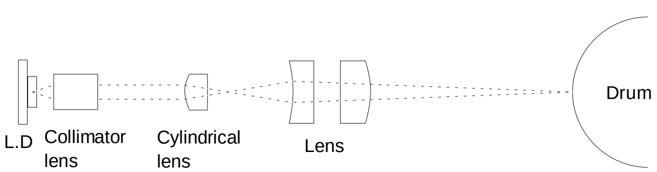
LSU internal structure





Side view





Sub scanning direction

Functions of major parts

① Collimator lens

Converges laser beams into parallel beams.

② Cylindrical lens

Corrects laser beams in the sub scanning direction by shift of the surface of the polygon mirror.

③ BD (Mirror, lens, PWB)

Detects the start timing of the laser scanning.

④ fθ lens

- Converges laser beams on a spot on the OPC drum.
- Equalizes the scanning speeds of laser beams at both ends and at the center.

⑤ Polygon mirror, polygon motor

Reflects laser beams at constant rotation.

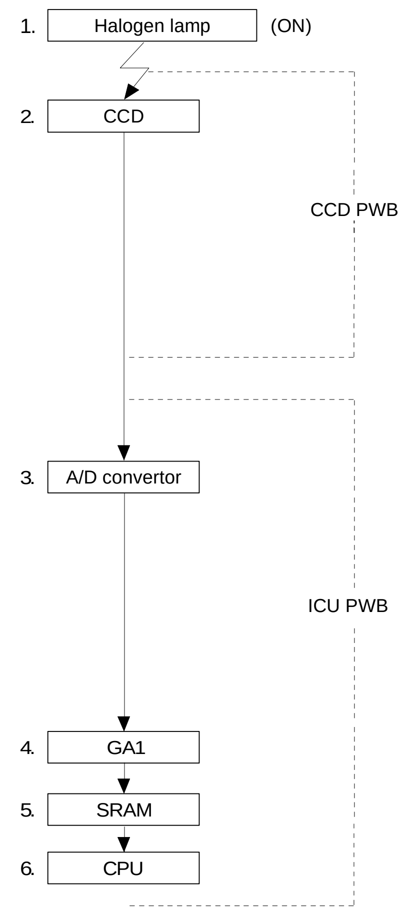
⑥ Semiconductor laser

Generates laser beams.

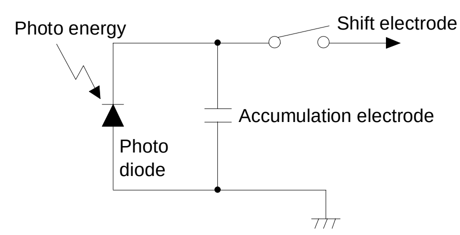
5. Image process section

Data flow (flowchart) | Content

<Lamp light quantity adjustment>

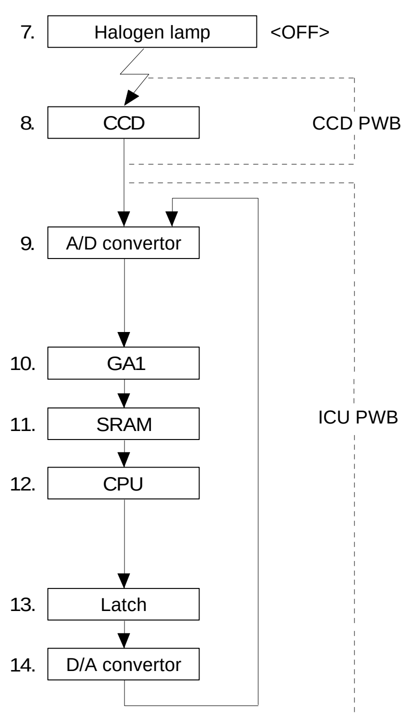


1. Halogen lamp (145W)
   The lamp is lighted by the DC power under the reference white plate.
2. 400dpi reduction line sensor (CCD)
   The sensor receives the reflected light as photo energy from the shading plate (reference white plate), and converts it into electrical energy (analog voltage).
   ⇓



3. A/D convertor
   The analog voltage is divided into 256 to convert into digital data, that is, the voltage is converted into binary 8-bit data.
   ⇓
   Actually, the white data before A/D conversion is about 4.0V, and the black data is about 1.1V. Therefore, the difference between about 4.0V of white and about 1.1V of black is divided into 256 divisions to convert into digital data.
   (Example: 1.1V → 0, 4.0V → 256, 2.55V → 128)
4. Gate array
   The digital data sent from the A/D convertor are inputted to the gate array temporarily.
5. SRAM
   Stores the data.
6. CPU
   Judges with the value written into the SRAM whether the light is too bright or too dark. If the light is too bright, it decreases the halogen lamp voltage. If the light is too dark, it increases the halogen lamp voltage. Procedures 1 ~ 6 are repeated to set the light quantity at the optimum level.

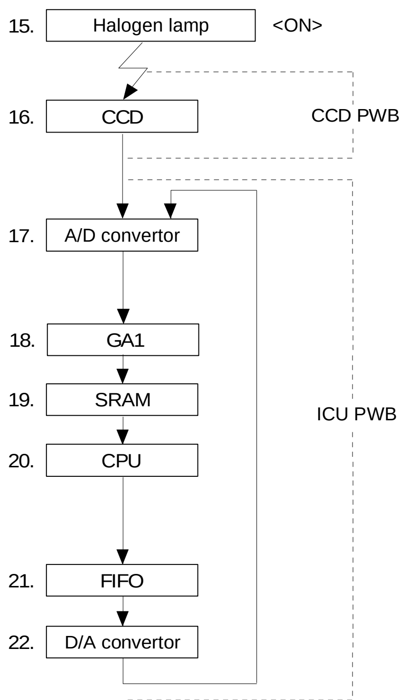
<Black level correction>



7. Halogen lamp (Black level correction)
   For black level correction, data obtained by SIM 63-2 are used. (The data are stored in the SRAM.)
8. CCD
   Though the halogen lamp is off, a constant voltage is outputted from the CCD.
9. A/D convertor
   The output voltage (analog voltage) is converted into a digital value. (The digital value may be ideally zero, however it will not become zero because of variations between machines.)
10. Gate array 1
    The digital data sent from the A/D convertor are temporarily stored in gate array 1.
11. SRAM
    Stores data.
12. CPU
    Obtains the optimum black reference value from the black image data written into the SRAM. In the hardware, the odd number pixels and the even number pixels in the main scanning direction are treated in two separate channels. Therefore, two reference values for the odd numbers and the even numbers are required.
13. Latch
    The reference values of the odd numbers and the even numbers are stored in the latch.
14. D/A convertor
    The black reference values stored in the latch are converted into analog voltages by the D/A convertor.
    The analog voltages are used as the black reference values (- reference) of A/D conversion.
    Procedures 8 ~ 14 are repeated to obtain the optimum black reference values.

Data flow (flowchart)	Content

<White level correction>



15. Halogen lamp
For white level correction, the halogen lamp is lighted at the voltage obtained in the light quantity adjustment under the shading plate and the shading plate is scanned.

16. CCD
The reflected light from the shading plate is received by the CCD as photo energy and converted into electrical energy (analog voltage).

17. The analog voltage is divided into 256 sections (0 ~ 255) to be digital data.

18. Gate array 1
The digital data are inputted to gate array 1 and thinned out every 16 lines.

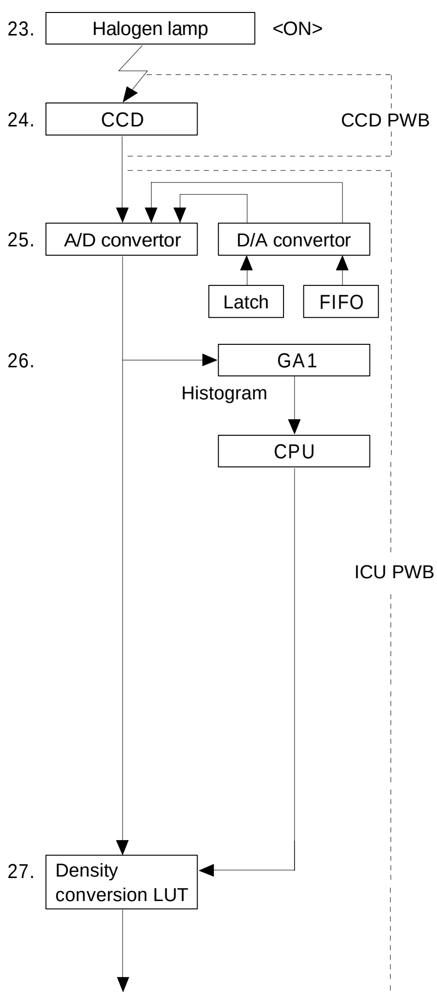
19. SRAM
Stores data. Thinning out every 16 lines is performed in order to minimize the bad effect by dirt on the shading plate.

20. CPU
The optimum white reference of 5048 pixels in the main scanning direction is obtained from the SRAM data. At that time, the correction of variations between odd/even numbers is performed as well as the correction of the halogen lamp and the lens. These corrections are made in order to prevent against darkness at both ends. In addition, the correction for variations between the document surface and the shading plate previously obtained by SIM 63-2 is performed.

21. FIFO
The correction data of one line are stored in the line memory (FIFO).

22. D/A convertor
The correction data of FIFO are converted into analog values to be the white reference value (+ reference) in 17. The white reference value is switched for every pixel.

<Document scanning>

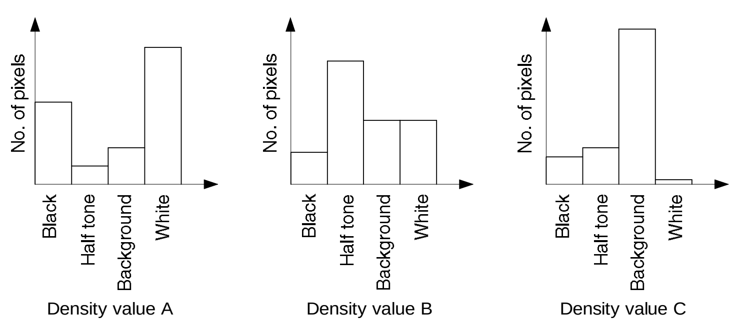


23. Halogen lamp
The halogen lamp is lighted at the voltage obtained by procedures 1 ~ 6 to radiate the document.

24. CCD
The scanned image data are sent to the ICU PWB with the analog signals.

25. A/D convertor, D/A convertor, latch, FIFO
Procedures 1 ~ 22 are performed at the specified timings such as turning on the power. The values obtained in 1 ~ 22, however, the black reference values of odd/even numbers are stored in the latch, and the white reference value is stored in the FIFO.
Therefore, shading correction is performed in copying. The white/black reference values of the A/D convertor are switched for every pixel to correct unevenness of the optical system and converted into digital values.

26. Gate array 1
Takes data of the density level of the scanned document.



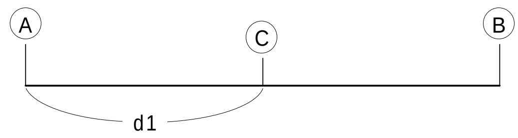
A judgment is made whether the document is of A type (an document of characters with much white area) or of B type (a photo document with much half tone area) or of C type (newspapers with much background area) to select the most suitable look-up table for density conversion.

27. CPU/SRAM
Converts the density.
For an document of A type, an LUT (look-up table) which provides clear characters is selected. For an document of B type, an LUT which provides clear half tone images is selected. For an document of C type, an LUT which removes background. Since process is performed for every several lines. the most suitable LUT may not be selected for some documents. In that case, the manual exposure mode is selected.

Data flow (flowchart)	Content

28. FIFO
Image data of one line are stored in the line memory (FIFO). This FIFO is for zooming. For reduction, the scanned image data are thinned out when they are written into the FIFO. For enlargement, the scanned image values are used as the values of plural pixels of the next one.

29. Gate array 2
Gate array 2 outputs the control signal to the FIFO to perform reduction and enlargement. Interpolation is also performed, which eliminates notches generated in enlargement. Two neighboring pixels before enlargement are interpolated primarily to eliminate notches.



(D5)(D6) : Density of pixel in normal ratio (0 ~ 255)

d1: Position if a pixel to be inserted.

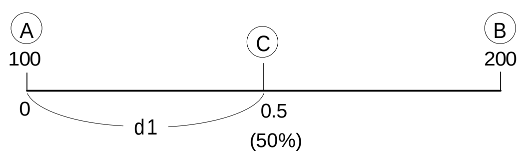
C: Density of the pixel which was formed by interpolation. (0 ~ 255)

⇓

C: $(1 - d1) \times$ (D5) $+ d1 \times$ (D6)

Example 1: Calculation of interpolation

Supposing that the density of (D5) at the normal ratio is 100 and that the density of (D6) is 200, and that the position of new pixel C after zooming is at 50% position, the density of C is as shown below.



(D7) $= (1 - 0.5) \times 100 + 0.5 \times 200$

↓ d1 ↓ A ↓ d1 ↓ B

= 150

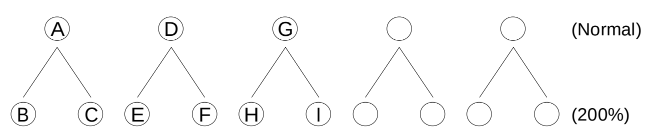
↓

Density of new pixel C

Example 2: In the case of enlargement

In the case of enlargement of 200%, the image process is made so that the number of pixels will be twice as greater as the number of the scanned pixels.

In short, the number of pixels scanned in the normal mode is duplicated to enlarge to 200%. One pixel in the normal mode is duplicated to two pixels in 200%. (Refer to the description below.)

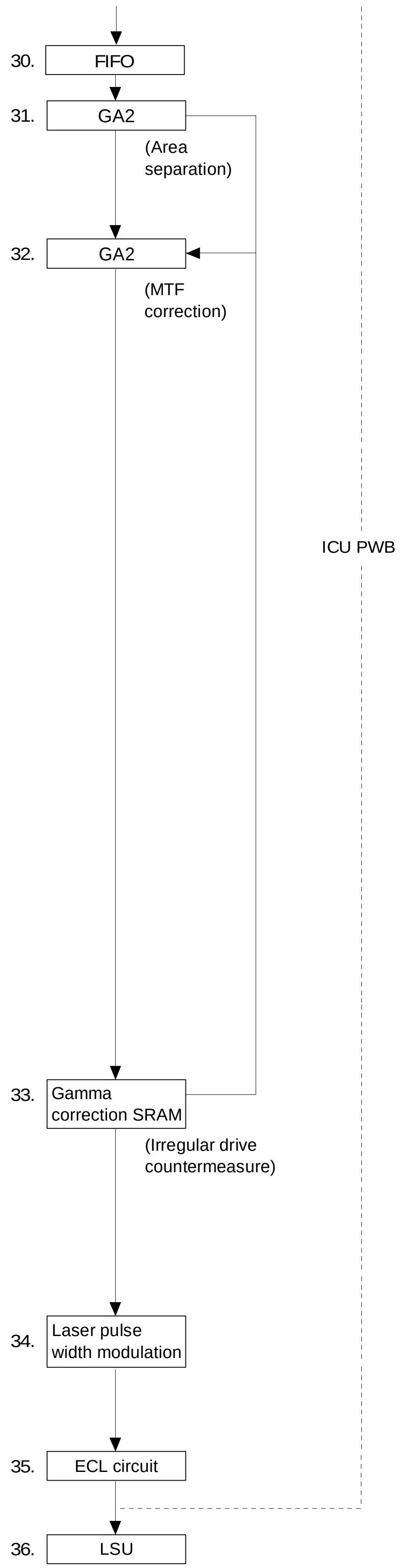


Then the density of pixels newly formed in the image process is determined. As shown in example 1, the position of newly made pixel is at the center (50% position) of two pixels scanned in the normal mode and the primary interpolation is performed as follows:

Ⓐ = Ⓑ Ⓒ = $\frac{Ⓐ + Ⓓ}{2}$ Ⓔ = Ⓓ Ⓕ = $\frac{Ⓓ + Ⓖ}{2}$

In the image process, enlargement is performed only in the main scanning direction. In the sub scanning direction, the scanning sped of the optical system is changed to perform enlargement. (For example in 200% enlargement, the scanning speed is changed to 1/2, and 50% enlargement is performed by duplicating the scanning speed.) The main scanning is performed by image process, and the sub scanning by varying the speed of the optical system. Zooming in the main scanning direction is separately performed from zooming in the sub scanning direction.

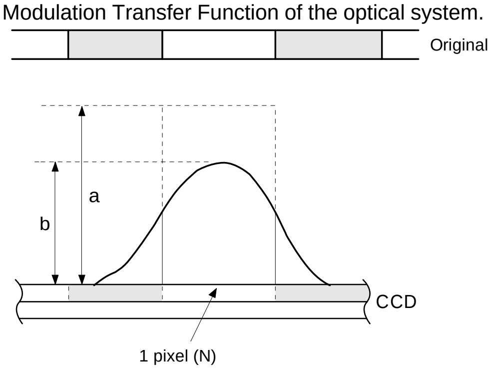
Data flow (flowchart)	Content



30. FIFO
This line memory (FIFO) is used for area separation and MTF correction.

31. Gate array 2
Performs area separation. In area separation, the characteristics of the target pixel and the neighboring pixels are judged to perform the optimum process. For example, judgement is made to identify that the area is a photo area or a hatched area such as newspaper photos.

32. Gate array 2
Corrects blurs in images in the main scanning direction and the sub scanning direction. Details are as follows.
MTF meas Modulation Transfer Function of the optical system.



a: Theoretical value
b: Value received by the CCD element (N)
The optical system provides out of focus even the focus adjustment is perfectly completed. When the CCD elements receive reflected light from the document, the light leaks to the neighboring pixels by the optical system characteristics. On the contrary, light come in from the neighboring pixels. Correction is made by adding the leaked lights and subtracting the lights from the neighboring pixels. This correction is called the MTF correction.
(In actual, this process includes calculation of the effect on the pixels by the preceding and the following lines.
The MTF correction performs process to provide clear characters by edge emphasis if the area separation result is a character area, and to provide less emphasis if the result is a hatched area, and to provide smooth images if the result is a photo area.
When the soft photo mode is selected, the area separation and the MTF correction are not performed, but the multi-value dithering is performed instead. The size of dither matrix in multi-value dithering can be selected by simulation.

33. Gamma correction SRAM
Gamma correction is performed to make optimum copying of image data. In the photo mode, gamma correction is made to reproduce clear half tone images. In the manual mode, gamma correction is performed to provide clear copying of characters.
Image data before correction are of 8 bit as well as image data after correction. (0 ~ 255)
In the photo mode, line alignment is performed, where the gamma correction curve of the odd number pixels and the even number pixels in the main scanning direction are changed to reduce fluctuations in drive of the machine.
In combination with the above area separation, it reduces bad effects of line alignment process for hatched documents.
The gamma correction SRAM performs the highlight process.

34. Laser pulse width modulation
The image data which are subjected to the gamma correction are converted into laser pulse signals (which varies the laser radiating time for each pixel.)
Radiating time of laser can be changed in the unit of 1/256.

35. ECL circuit
The laser pulse width signal is sent to the LSU at ECL level.

36. LSU
The laser scan unit performs printing.

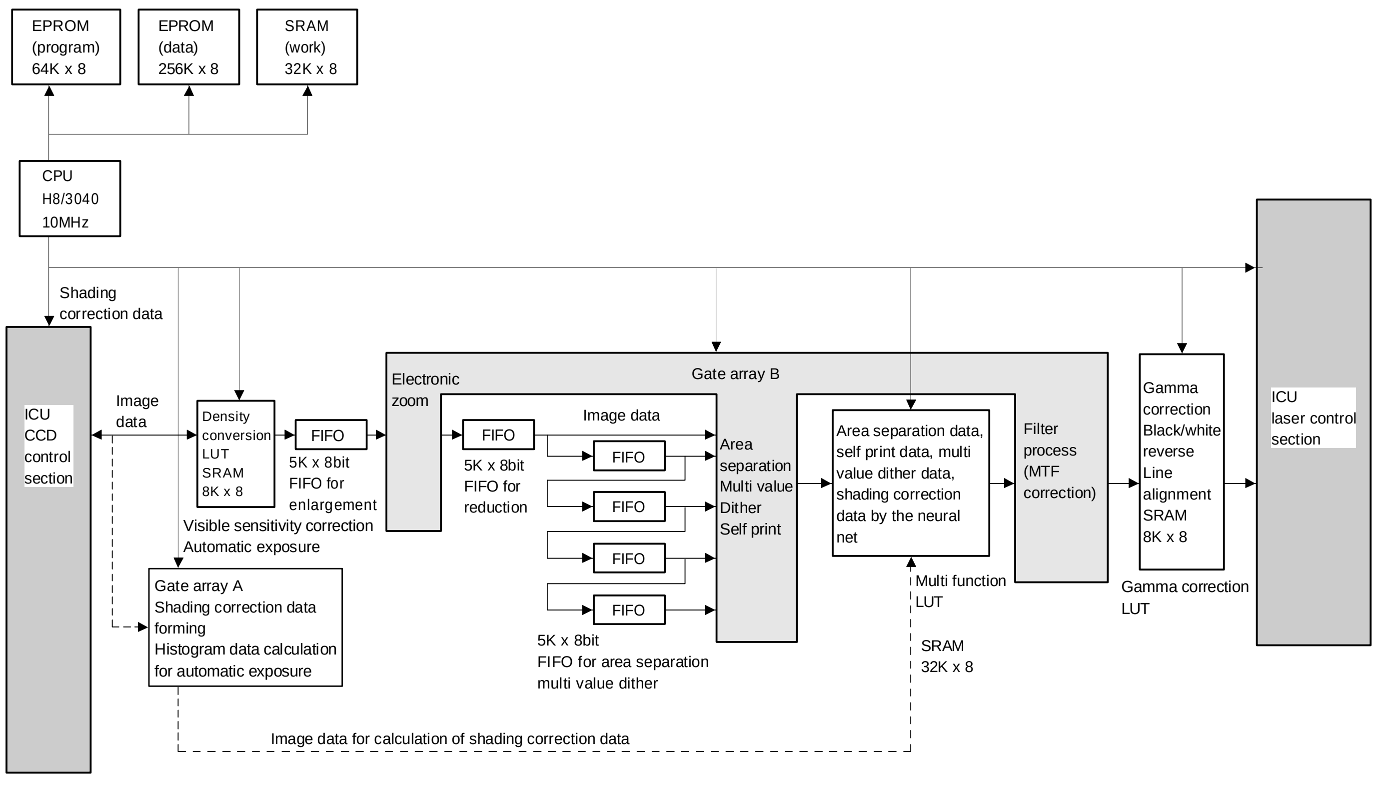
(2) Image process section

The image process section is composed of gate arrays A and B, the CPU, and memories (SRAM, FIFO, EPROM). Gate array A forms data for shading correction and calculates histogram data for automatic exposure. Gate array B performs area separation, filter process, address generation for self printing, multi-value dithering, and electronic zooming of main scanning.

The CPU performs register setting and rewriting of LUT (look up table) every time when the user changes the mode. It also calculates the correction value of shading correction.

The figure below shows the flow of image signals.

ICU image process section block diagram



[Shading correction]

The analog image data from the CCD PWB are inputted to the CCD control section in the ICU and converted into digital data, and passed through gate array A in the ICU image process section, and written into the multi-function LUT (Look Up Table). (Path shown with dotted line in the above diagram.)

Gate array A performs thinning out of 16 lines at that time. Thinning out of 16 lines is performed when there is dirt on the shading plate.

[Auto exposure]

The analog image data from the CCD PWB are inputted to the CCD control section in the ICU and corrected by the shading data obtained from the above method and converted into digital data and inputted to gate array A. In gate array A, the total number data (simple histogram) of pixels in each density is calculated as shown in 1-5. The calculated data are used to judge that the document is of background type such as newspapers or of half tone type such as photos or of white type with less black and without half tone such as character documents. The data are calculated for each line. According to the data, the CPU selects the most suitable density conversion look up table from 32 kinds of density conversions look up tables in the density conversion LUT.

[Electronic zooming]

The image data, after auto exposure and the visual sensitivity correction, are written into the FIFO for enlargement. Gate array B controls the enable signal for reading the enlargement FIFO to thin out the read data, enlarging images. For example, in enlargement of 200%, the read enable signal is provided for every pixel to make enlargement. The image data thinned out for enlargement are inputted to gate array B and the primary interpolation is performed as shown in 1-6. (For details, refer to 1-6.) The image data thinned out primarily are written into the reduction FIFO. The enable signal for writing is controlled to thin out for reduction.

[Area separation]

After electronic zooming, the image data are written into the FIFO for area separation/filter/multi-value dithering. There are four FIFO's and each one sends data for one line. Therefore gate array B can input image data of five lines. Gate array B calculates the characteristic value of peripheral pixels according to the image data of five lines and the result is outputted to the address of the multi-function LUT. The multi-function LUT is the same one described in the shading correction. When the are separation mode is selected, the CPU reads the data for area separation from the EPROM (for data) and write into the multi-function LUT.

[MTF correction]

When the characteristic value outputted from gate array B is inputted to the address of multi-function LUT, data which show the characteristics of the peripheral pixels are outputted from the multi-function LUT. For example, the data show that the pixel and the peripherals are characters and edged of line drawing or that they are part of a hatched image of photo in a newspaper or that they are part of a photo of continuous gradation (that is not a hatched photo). Filter process is performed according to each pixel's characteristics.

[Gamma correction/line alignment/black-white highlight]

After the MTF correction, the image is subject to the gamma correction in order to cope with the OPC drum characteristics, the developing characteristics, and the actual copy density. Before copying, the CPU reads the density conversion look up table value corresponding to the value which was set by the user with the density adjustment key from the EPROM (data), and writes the data into the gamma correction LUT (SRAM). The image data are connected to the lower 8 bits of the gamma correction LUT address and converted by the look up table. Black-white highlight is performed at the same time.

[Soft photo mode]

This is the multi-value dithering mode which has been newly added from this mode. The area gradation is combined with the pulse width modulation to improve the gradation of photo. The size of area gradation (dither matrix) can be selected with simulation.

[Self printing mode]

Gate array B prints out the test pattern by outputting the address count values of main scanning and sub scanning.

Gate array A

Pin arrangement table

No.	Pin name	I/O	Function
1	GND		
2 ~ 7	RAMADR0 ~ RAMADR5	O ~ O	Data bus to the peripheral memory connected to this LSI.
8	VDD		
9	RAMADR6	O	Data bus to the peripheral memory connected to this LSI.
10	RAMADR7	O	
11	GND		
12	RAMADR8	O	Data bus to the peripheral memory connected to this LSI.
13	GND		
14	VDD		
15 ~ 20	RAMADR9 ~ RAMADR14	O ~ O	Data bus to the peripheral memory connected to this LSI.
21	FINAL	O	Signal which shows the end of shading correction.
22	GND		
23 ~ 30	RAMADR0 ~ RAMADR7	I/O ~ I/O	Address bus to the peripheral memory connected to this LSI.
31	GND		
32 ~ 42	XIFDAT0 ~ XIFDAT7	I/O ~ I/O	Data bus to set the built-in register.
43	GND		
44 ~ 53	SHADOUT0 ~ SHADOUT7	I/O ~ I/O	Signal to output the data after shading correction.
54	GND		

No.	Pin name	I/O	Function
55 ~ 60	XIFADR0 ~ XIFADR5	IN ~ IN	Data bus to set the built-in register.
61	RAMRD	OUT	Read signal to the peripheral memory.
62	VDD		
63	GND		
64	WCLK	OUT	Not used.
65	CLK1	IN	System clock of this LSI. Clock of 16MHz is inputted.
66	XIFEN	IN	Data enable signal to the built-in register.
67	XIFRD	IN	Data read signal to the built-in register.
68	XIFWR	IN	Data write signal to the built-in register.
69	RESET	IN	Initializes the LSI.
70	VDD		
71	CLK2	IN	System clock of this LSI. Clock of 16MHz is inputted.
72	RAMWR	OUT	Write signal to the peripheral memory
73	HSYNC	IN	Image data 1 line read start signal.
74	PAGE	IN	Signal which shows the effective area of one page of image data.
75	RESERVE		Not used.
76	RESERVE		
77	RESERVE		
78	RESERVE		
79	GND		
80	RESERVE		Not used.
81	RESERVE		
82	RESERVE		
83	RESERVE		
84	GND		
85 ~ 87	H0 ~ H2	OUT ~ OUT	Not used.
88	VDD		
89	GND		
90 ~ 92	V0 ~ V2	OUT ~ OUT	Not used.
93 ~ 100	ADIN0 ~ ADIN7	IN ~ IN	Image data bus

Gate array B

Pin arrangement table

No.	Pin name	I/O	Function
1	GND		
2	VCC		
3 ~ 10	AIN0 ~ AIN7	IN ~ IN	(n) Line image data input pin.
11 ~ 14	RAMADR0 ~ RAMADR3	OUT ~ OUT	Signals according to each mode such as the result of area separation are outputted to the external LUT from this pin.
15	GND		
16 ~ 19	RAMADR4 ~ RAMADR7	OUT ~ OUT	Signals according to each mode such as the result of area separation are outputted to the external LUT from this pin.
20	VCC (fixed)		
211	GND (fixed)		
22	GND		
23 ~ 30	BIN0 ~ BIN7	IN ~ IN	(n+1)the line image data input pin
31	RESERVED		Not used.
32 ~ 34	RAMADR8 ~ RAMADR10	OUT ~ OUT	Signals according to each mode such as the result of area separation are outputted to the external LUT from this pin.
35	GND		
36 ~ 39	RAMADR11 ~ RAMADR14	OUT ~ OUT	Signals according to each mode such as the result of area separation are outputted to the external LUT from this pin.
40	GND		
41 ~ 48	RAMDATA0 ~ RAMDATA7	IN ~ IN	Pin for data input from the external LUT.
49 ~ 52	FILOUT0 ~ FILOUT7	OUT ~ OUT	Pin for output of the result of filter process.
53	GND		
54 ~ 57	FILOUT4 ~ FILOUT7	OUT ~ OUT	Pin for output of the result of filter process.
58	CLK1	IN	Clock signal input pin. Clock of 16MHz is inputted.
59	GND		
60	VCC		
61	GND (fixed)		
62	VCC (fixed)		
63 ~ 70	CIN0 ~ CIN7	IN ~ IN	(n+2)the line image data input pin
71 ~ 78	XIFDAT0 ~ XIFDAT7	I/O ~ I/O	Data bus to set the built-in register.
79	GND		
80 ~ 87	DIN0 ~ DIN7	IN ~ IN	(n+3)the line image data input pin
88	RESET	IN	Reset signal of the LSI
89 ~ 94	XIFADR0 ~ XIFADR5	IN ~ IN	Address bus to select the built-in register.
95	AREALDLY	OUT	Signal showing the effective image area which is behind from AREA signal by 4 clocks. LOW active.
96	CLK2	IN	Clock signal input pin. Clock of 16MHz is inputted.
97	XIFRD	IN	Data read signal to the built-in register. LOW active.
98	XIFWR	IN	Data write signal to the built-in register. LOW active.
99	XIFEN	IN	Data enable signal to the built-in register. LOW active.
100	VCC (fixed)		
101	GND (fixed)		
102 ~ 105	BUNRIOUT0 ~ BUNRIOUT3	OUT ~ OUT	Area separation test pin.
106	GND		
107 ~ 112	BUNRIOUT4 ~ BUNRIOUT9	OUT ~ OUT	Area separation test pin.
113	GND		
114	CLK3	IN	Clock signal input pin. Clock of 16MHz is inputted.
115 ~ 125	ZOOMIN0 ~ ZOOMIN10	IN ~ IN	Zooming process data input pin.
126	GND		
127 ~ 130	ZOOMOUT0 ~ ZOOMOUT3	IN ~ IN	Zooming process data input pin.
131	GND		
132 ~ 135	ZOOMOUT4 ~ ZOOMOUT7	IN ~ IN	Zooming process data input pin.
136	GND		
137	VCC		
138 ~ 140	ZOOMOUT8 ~ ZOOMOUT10	IN ~ IN	Zooming process data input pin.
141	FIFOWEN	OUT	Write enable signal to the line memory. LOW active.
142	VCC (fixed)		
143	GND (fixed)		
144	GND		
145	FIFOREN	OUT	Read enable signal to the line memory. LOW active.
146 ~ 148	RAMDLY0 ~ RAMDLY2	OUT ~ OUT	10-clock behind signal of RAMDATA0 ~ 2.
149	AREAHDLY	OUT	Signal showing the effective image area which is behind from AREA signal by 5 clocks. LOW active.
150	HSYNC	IN	Image data 1 line scanning start signal
151	AREA	OUT	Signal which shows the effective image area. LOW active.
152 ~ 159	EIN0 ~ EIN7	IN ~ IN	(n+4)the line image data input pin.
160	PAGE	IN	Signal which shows one page of image data. LOW active.

[2] PROCESS SECTION

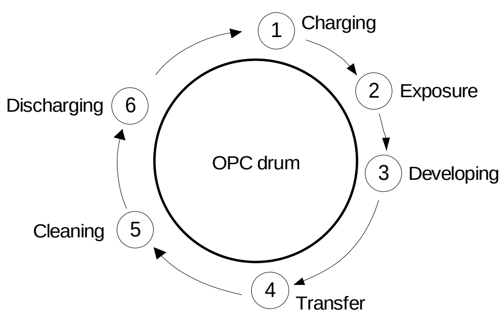
(OPC drum, cleaning unit)

1. Outline

The indirect electrostatic copiers use normal paper for copying, and form electrostatic latent images on the OPC drum surface which can be used repeatedly, develop them into visible images (toner images), and transfer them on copy paper. Copies are made indirectly in the copier of this type.

The PPC (Plain Paper Copier) makes copies in six processes: charging, exposure, developing, transfer, discharging, and cleaning which cleans the OPC drum surface to use is repeatedly after transfer.

(1) Image forming process



① The OPC drum is charged.

② The OPC drum is exposed to form electrostatic latent images.

③ Toner is attracted to the electrostatic latent images.

④ The developed toner images are transferred on recording media such as paper.

⑤ Residual toner remaining on the OPC drum surface is cleaned.

⑥ Residual charges on the OPC drum are removed.

(2) OPC drum

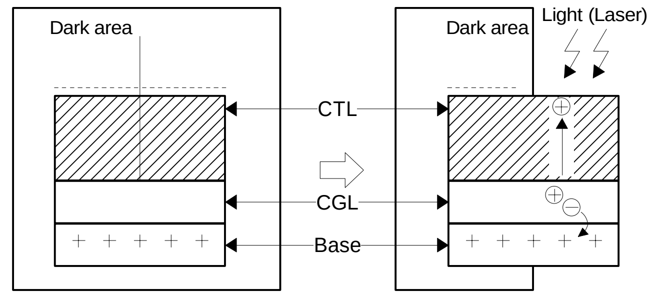
Some materials conduct electricity, and some others do not. The materials are divided into three groups according to their conductivity: conductors, semiconductors, and insulators.

This classification is not strict, and it is difficult to classify the materials strictly.

Generally speaking, the materials with resistivity of 10^8 Ω cm or above are called insulators. Those with resistivity of 10^{-3} Ω cm or below are called conductors.

The materials between the two are generically called semiconductors. The conductors are always conductive. The semiconductors are normally not conductive, but under a certain condition become conductive.

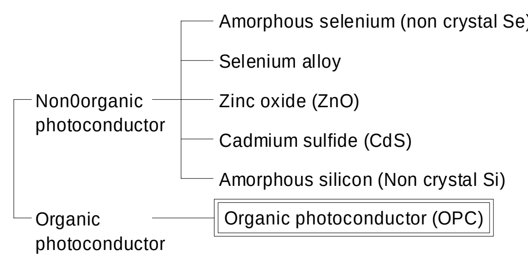
The photoconductor used in the copiers are insulators when they are not exposed with light, and reduce the resistivity when they are exposed with light, that is, they become conductive (by the photo conductivity phenomenon) when exposed with light. They are also called as photo semiconductors and used in the copiers.



Principle of photoconductor (conductivity)

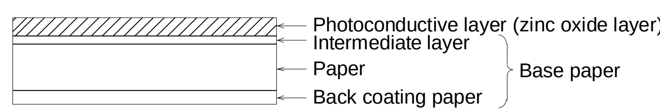
(3) Kinds of photoconductors

Major photo conductive materials used in the copiers are zinc oxide (ZnO), amorphous selenium (amorphous Se) alloy, cadmium sulfide (CdS), amorphous silicon (amorphous Si), and organic photoconductor (OPC).

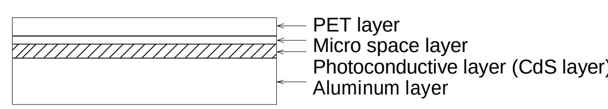


The compositions of photoconductors used in the copiers are shown below.

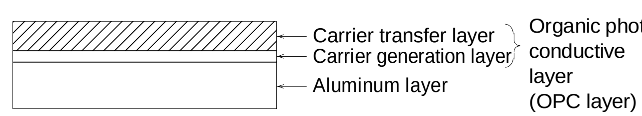
Zinc oxide (ZnO) master



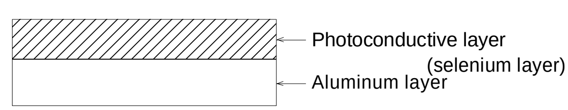
Cadmium sulfide (CdS) drum



Organic photoconductor (OPC) master or drum



Selenium (Se) drum)



Characteristics of organic photoconductors (OPC)

- Can be formed into various shapes (drum, sheet, belt)
- High insulation in a dark place. (Acceptability and retainability of charges)
- Light weight
- Stable against humidity and temperature
- Safe and clean to the environment (harmless)
- Weak in wear by friction
- Weak in durability against light and ozone

(4) Characteristics of photoconductors

The important characteristics of photoconductors are as follows:

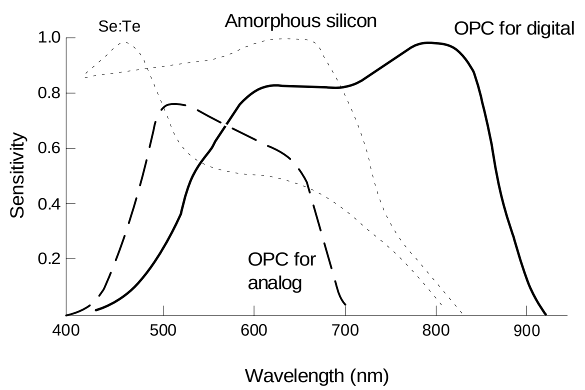
1. Photo sensitivity
2. Spectrum characteristics
3. Acceptance potential
4. Charge retainability
5. Residual potential
6. Fatigue

[Photo sensitivity]

It is determined by the attenuation speed of the potential when exposed with light.

[Spectrum characteristics]

The sensitivity of photoconductors differs depending on the kind and the waveform of light.



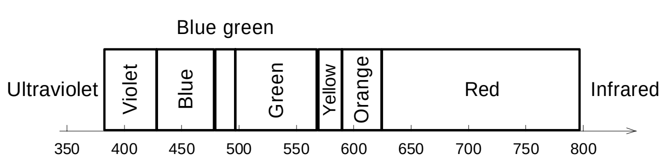
Spectrum sensitivity

Relationship between color and waveform

Human eyes can feel the lights with waveform of 380nm to 780nm.

These are called "Visible lights." The light whose waveform is shorter than that is called "Ultraviolet light." The light whose waveform is longer than that is called "Infrared light."

The figure below shows the relationship between lights and waveforms.



[Acceptance potential]

The dark resistance of the photoconductor layer decreases as the electric field applied between layers increases.

When the photoconductor is charged, the electric field is formed to a high level and the resistance of the layer decreases to restrict the charging amount of the photoconductor. The potential of the photoconductor at that time is called the acceptance potential, which serves as an important factor to determine the potential contrast. The photoconductor is generally charged to a potential slightly lower than the acceptance potential in order to avoid applying an electrical strain to the photoconductor.

[Charge retainability]

The retaining time of electrostatic latent images on the photoconductor is determined by the speed of decrease in the potential in a dark place. That is, it is measured with the time for the photoconductor potential to decrease to the half of the initial level. This retainability of electrical charge makes a problem when the interval time between exposure and developing is longer. In the machines where a series of operations of charging, exposure, and developing are automated, the interval between the processes is short enough and there is no problem.

[Residual potential]

When the charged photoconductor is exposed, the potential is rapidly attenuated at first then slowly. The potential where this slow attenuation starts is called the residual potential. The lower the residual potential is, the greater the voltage contrast is. Therefore, the lower residual potential is desirable.

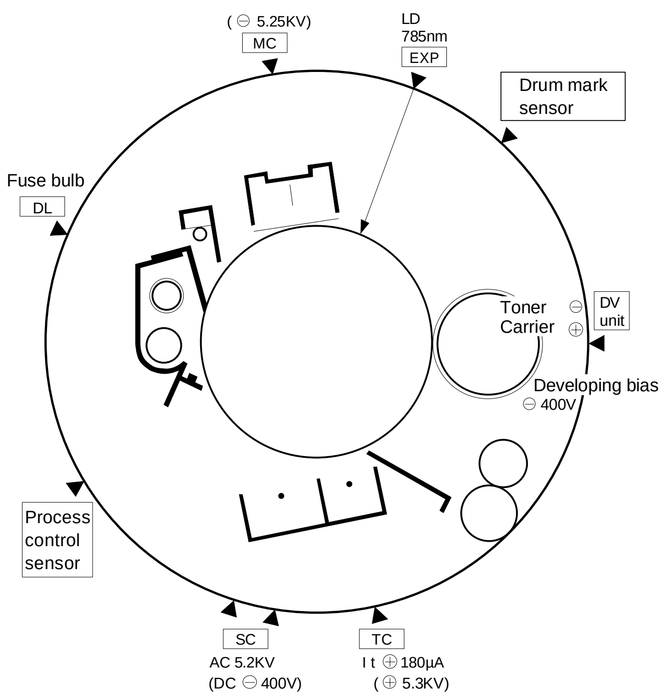
[Fatigue]

When the photoconductor is charged and exposed repeatedly, it is fatigued. Fatigue of the photoconductor results in increase in attenuation speed of the photoconductor potential and decrease in the retainability of charges.

In the above, the necessary characteristics for the photoconductors are described. In an actual machine, when charging is repeated by the charger, dust and dirt or splashed toner may be attached to the saw tooth. These are not resulted from uneven charging, and they should be removed by cleaning.

2. Basic process and composition

- This machine employs the scorotron system to charge the photoconductor surface uniformly to a certain level. The conventional corona charger mechanism is employed which is composed of the corona wire and the saw tooth plate (stainless plate of 0.1mm thick).
  In corona charging, oxygen molecules in the air are ionized to form ozone. This mechanism suppresses the generation of ozone.
- The process separation mechanism is employed for serviceability.
- The one-touch stopper mechanism prevents against high voltage leakage caused by drop of the corona charger unit.



Drive system view

(1) Details of image forming process

Step 1: Charging

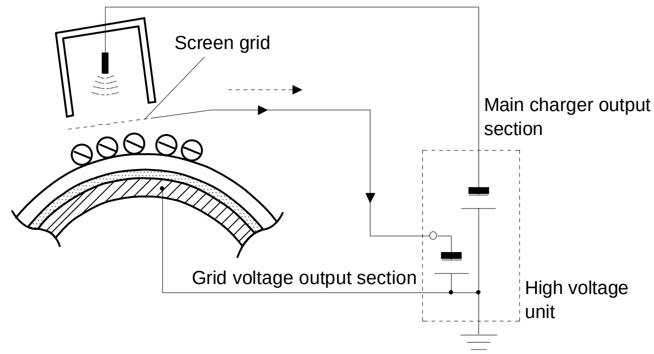
Main charger high voltage transformer (MHVG)

	Grid voltage	Developing bias voltage
Standard mode	–490V	–400V
Photo mode	–490V	–400V
TSM mode	–440V	–350V
Printer mode	–460V	–400V

A uniform negative charge is applied to the OPC drum surface by negative corona discharge of the main charger.

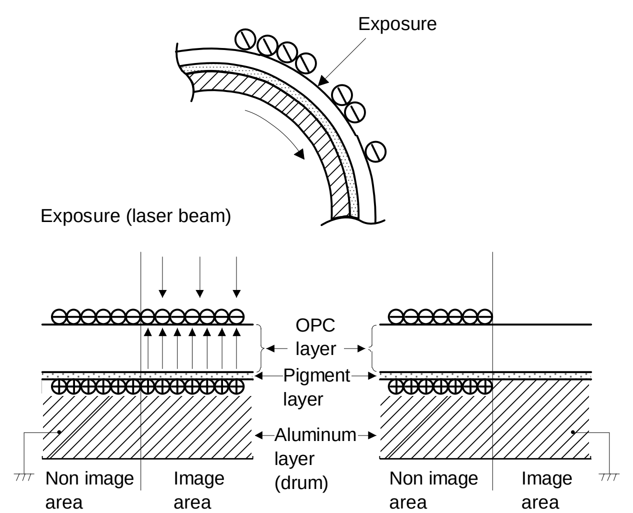
The OPC drum surface potential is controlled by the screen grid voltage to be virtually the same level as the grid voltage.

- When the drum surface potential is lower than the grid voltage, electric charges generated by discharging of the main charger are passed through the screen grid to keep charging until the drum surface potential reaches the same level as the grid voltage.
- When the drum surface potential reaches about the same level as the grid voltage, electric charges generated by discharging of the main charger flow through the electrode of the screen grid to the high voltage unit grid voltage output circuit. Therefore the drum surface potential is kept at the same level as the grid voltage.



Step 2: Exposure (laser beams)

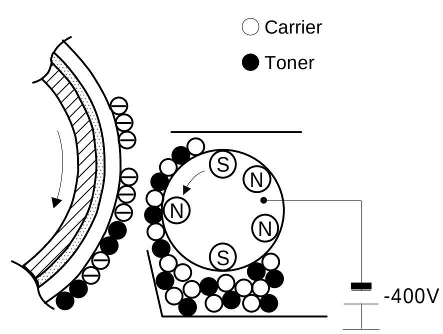
Laser beams are generated in the LSU according to the print signal from the ICU and radiated to the drum surface. The resistance of the are of OPC layer where laser beams are radiated reduces to discharge negative charges, forming electrostatic latent images on the drum surface.



Step 3: Developing (Bias –400V)

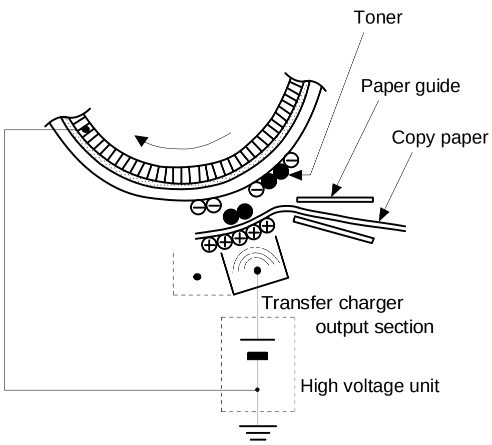
The electrostatic latent images on the drum surface are made visible images. This model uses the two-component magnetic brush developing system to supply the bias voltage of –400V to carriers (MG roller), and toner is negatively charged by friction with carriers.

Since the non-image area on the drum is negatively charged greater than the developing bias, the negatively charged toner is repulsed from the drum. The image area on the drum is exposed by laser beams and its potential is decreased. Then negative toner is attached to it by the DV bias.



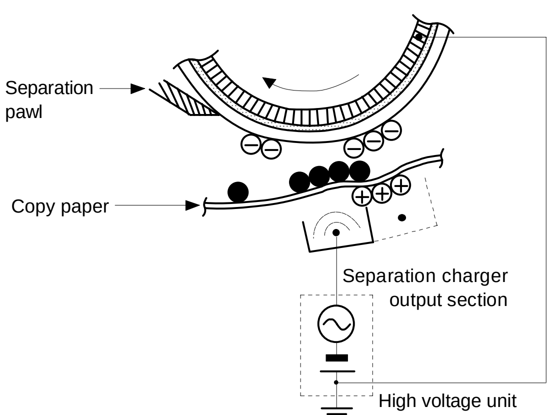
Step 4: Transfer

The visible images on the drum surface are transferred to copy paper. Positive corona of the transfer charger is applied to the back of the copy paper to transfer toner on the drum to the copy paper.



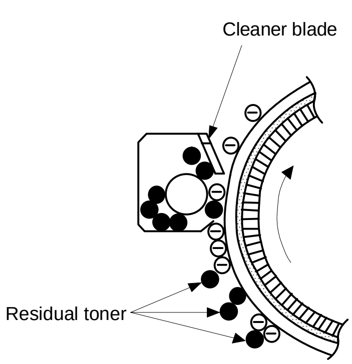
Step 5: Separation

Since the copy paper is positively charged and the drum is negatively charged after transfer, an attraction force is generated between the drum and the copy paper. Then an AC corona overlapped with negative DC is applied to the copy paper to decrease the copy paper potential to the same level as the drum surface potential. Therefore an attraction force between the drum and the copy paper disappears, and the copy paper is separated by its own flexibility. If the paper is not separated by the separation charger, it is forcibly separated by the separation pawl.



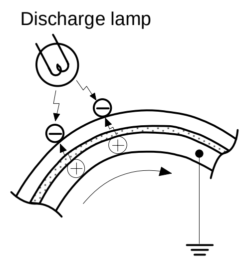
Step 6: Cleaning

Residual toner on the drum is removed by the cleaning blade.

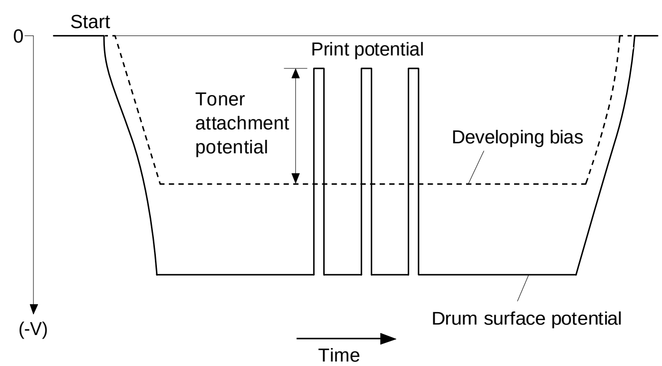


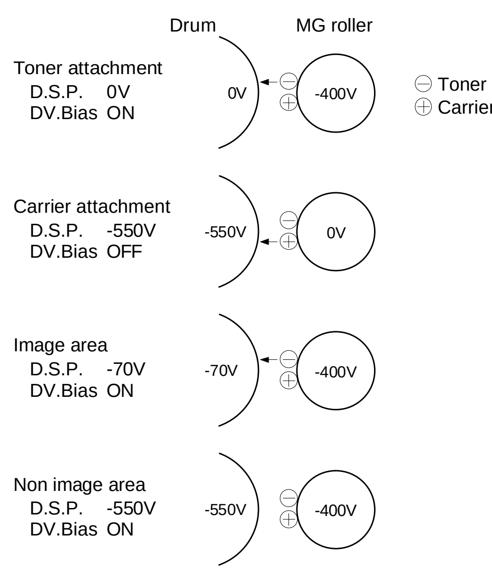
Step 7: Discharge

The discharge lamp light is radiated to the drum to reduce the electric resistance of the OPC layer, eliminating the residual charges.



(3) Potential transition of the DV unit section



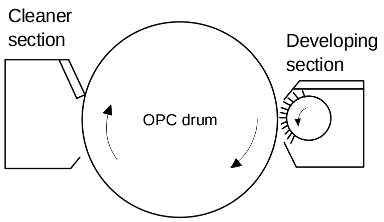


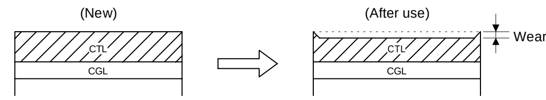
DSP: Drum surface potential

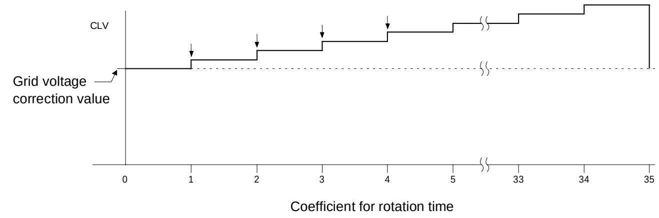
(4) OPC drum sensitivity reduction correction

In the AR-5132, deterioration of copy quality is prevented by correction with the charging grid voltage against the potential reduction of the OPC drum due to repeated use.

The drum wear increases the grid voltage to maintain the drum surface potential at a constant level, and the apparent sensitivity of the OPC drum is decreased. To correct this, the laser beam strength is increased when the coefficient of the drum rotating time for correction of the charging grid voltage reaches a certain level.





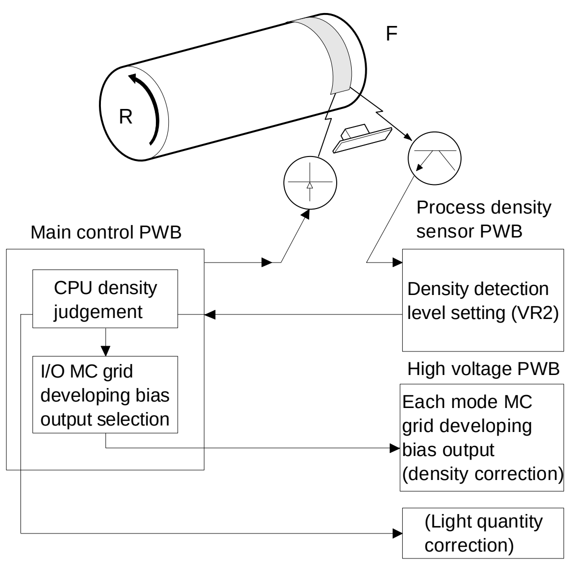


(5) Process control function

[Outline]

The density of the reference toner image formed on the OPC drum surface is used as the standard patch density, and the developing bias and the charging grid voltage are controlled to provide the same density as the standard patch density for stabilizing the copy images.

That is, the process conditions are set, and the high voltage output is changed and corrected so that the toner density is stabilized under the conditions.

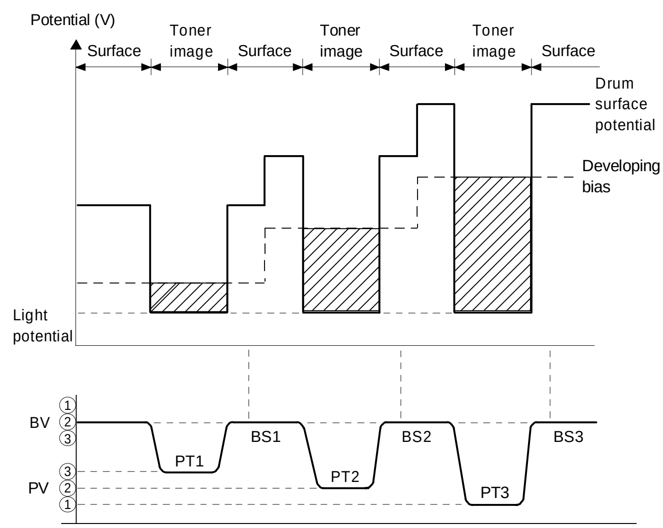


Process control

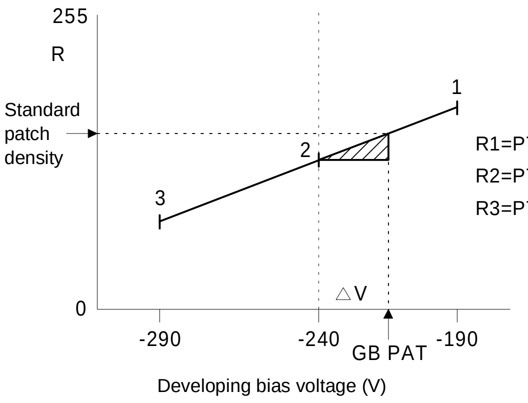
① Toner patch images are formed on the OPC drum surface under the three kinds of conditions (MC grid bias voltage) and the developing bias. (The voltage is an actually measured value.)

In the process control, toner patch images are formed at the laser output of the reference grid voltage (–410V) and the developing bias (–240V) ±50V and duty of 100%.

② The three kinds of toner patch images and the drum surface are measured with the process density sensor to obtain the relationship between them.



③ The developing bias voltage is obtained from comparison with the standard patch density.



In the AR-5132, the absolute value of the density sensor output value is not directly used for the control calculation, but the ratio of the drum surface sensor output value (BSn) and the toner patch image sensor output value (PTn) is used for the control calculation.

Since the ratio of PTn/BSn) is not affected by the change in the absolute value of the light quantity of the reflection type sensor due to dirt or deterioration, stable control is performed.

④ In the developing bias/MC grid voltage correction, the value of △V of the developing bias voltage calculated with the standard patch density and the process control is fed back to the bias voltage and the MC grid voltage in each mode.

When the developing bias voltage is corrected, the corresponding MC grid bias is calculated and controlled.

⑤ When a value reaching the reference level is not obtained in a series of control procedures, the patch forming conditions are shifted toward the reference level side and repeat the series of control procedures. The repetition is allowed for max. five times.

LD power correction

The LD power correction is performed depending on the result of the developing bias voltage calculation. When the correction width △V of the developing bias voltage becomes greater, the MC grid voltage is corrected accordingly. If the LD power is the same at that time, the apparent sensitivity of the OPC drum is changed. To correct this, the LD power is made greater when the developing bias voltage is increased; on the contrary the LD power is made smaller when the developing bias voltage is decreased. The width of decrease or increase is determined according to the built-in table. This correction stabilizes half tone prints.

Process control timing

In the AR-5132, the process control is performed at the following timing.

a. When the power switch is turned on. (during warming up)

b. When the accumulated copy time reaches 30 min, the process control will be made in the next copying.

c. When the standby time reaches 1 hour, the process control will be made in the next copying.

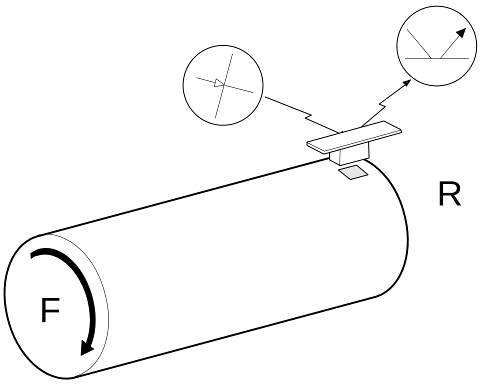
d. When simulation 46 is executed.

Drum marking

In the AR-5132, toner patch images are formed at the same position on the OPC drum to improve accuracy of the process control.

That is, a marking is provided on the drum, and the marking point is sensed and toner patch images are formed at a certain position.

If the marking is not sensed, the copy density is extremely reduced.



[3] DEVELOPING SECTION

1. Basic outline

(1) Two-component developer

Developer is composed of tow components; toner and carrier.

Carrier functions as a media to attract toner to electrostatic latent images on the OPC drum.

As the toner is mixed with the carrier, the friction changes it to positive or negative.

Developer characteristics changes due to deterioration to degrade print quality. Therefore developer must be replaced periodically.

(2) Two-component magnetic brush developing

A rotatable non-magnetic sleeve is provided on the magnet roller and rotated.

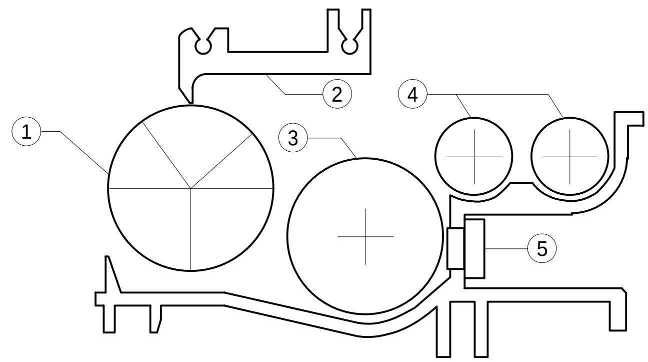
Carrier forms a magnetic brush on the sleeve surface by the magnetic force to attract toner to electrostatic latent images on the OPC drum.

(3) Developing bias

Since the reverse developing system is employed, toner is attracted to the area (light potential area) where laser beams are radiated. Though it is the light potential area, the OPC drum is negatively charged. To attract negatively charged toner to the OPC drum, a higher (absolute value) bias must be applied to the MG roller. Therefore, the amount of attracted toner can be varied by the level of the developing bias voltage.

The developing bias serves to prevents against attachment of excessive toner by setting it lower (in absolute value) than the surface potential (dark potential) when making white background.

2. Basic composition



No.	Name	
①	Developing magnet roller	Forms the magnetic brush of carrier by the magnetic force.
②	Developing doctor blade	Used of regulation of the magnetic brush height.
③	Developing stirring roller	Stirs carrier in the developing unit to distribute toner uniformly.
④	Developing transport roller	Transports toner supplied from the toner hopper unit to the stirring section.
⑤	Developing toner density sensor	Detects the toner density in the developer.

3. Basic operation

When the power switch of the machine is turned on, the machine starts warming up. After about one minute, the main motor rotates.

The drive power of the developing unit is transmitted from the main motor through the main drive unit to the developing drive unit.

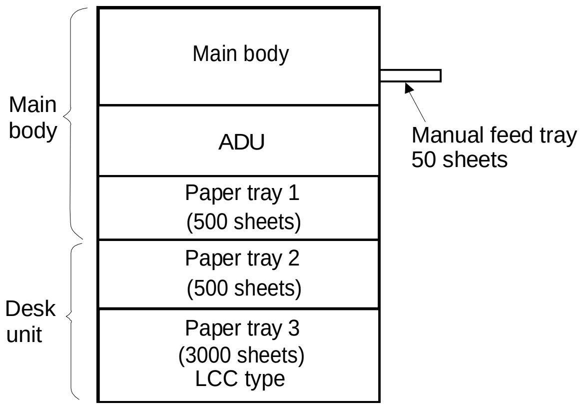
Change in the mixing ratio of toner and carrier is sensed by the toner density sensor in the developing unit as the change in magnetic permeability, and outputted to the analog input pin of the main PWB CPU of the main body.

The CPU monitors the input voltage level, and controls the main motor and toner motor to supply, transport, and stir toner until the proper density is obtained.

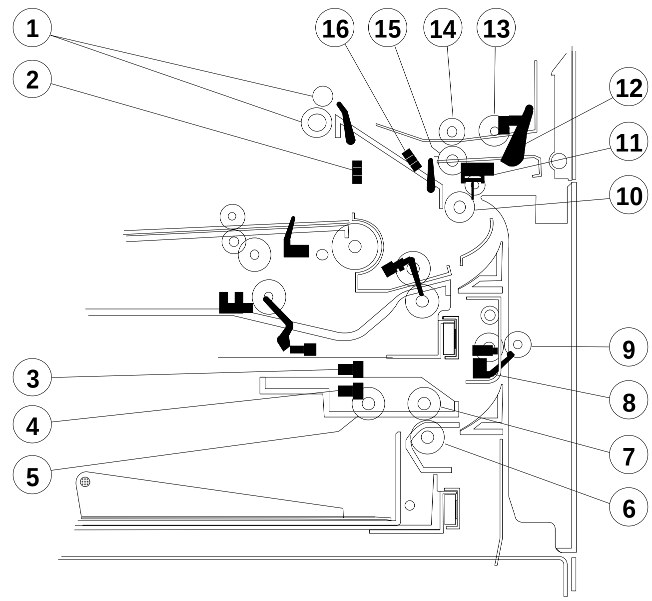
[4] PAPER FEED SECTION

1. Basic outline

The AR-5132 employs the font loading system and the multi paper feed table which can be stored inside the machine, cutting the installation space. It is also equipped with the two-step trays, the 3000-sheet LCC tray, and the manual paper feed tray which allows continuous feeding of 50 sheets as standard provisions.



2. Basic composition

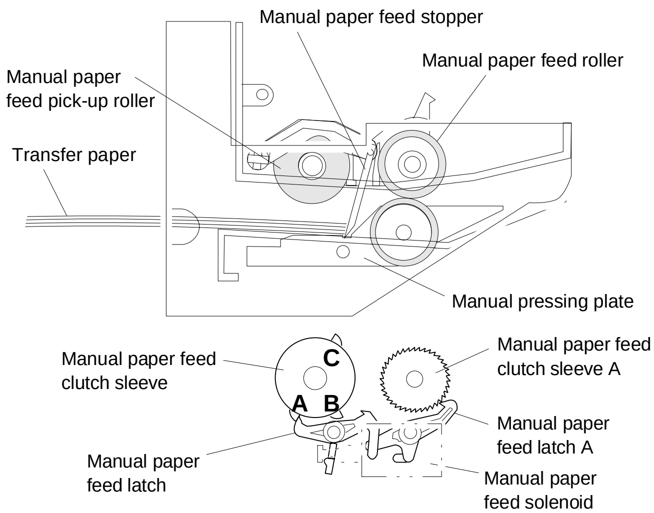


No.	Name	Function, operation
①	Resist roller	Makes synchronization between paper and images by control of the resist roller clutch.
②	(PPD2) Paper transport sensor	Used to control the transport roller clutch (TRC).
③	(LUD3) Lift upper limit sensor	Used to control the lift-up motor. Stopped at HIGH.
④	(PED3) Paper empty sensor	Used to detect paper empty.
⑤	Pick-up roller	Picks up paper and falls simultaneously with turning on the paper feedf solenoid.
⑥	Paper feed separation roller	Preents agaisnt multi paper feed.
⑦	Paper feed roller	Paper feed roller for the paper tray 1, (Includes the one-way clutch.)
⑧	(PID) Paper entry sensor	Detects pper entry from the paper tray 1 and turns off the paper feed solenoid.
⑨	Transport roller	Transports paper from the paper tray 1.
⑩	Transport roller	Transoprts paper from the cassette to the resist roller.
⑪	(TFD) Wast toner fll sensor	Full at LOW.
⑫	(PED1) Paper empty sensor	Detects paper empty in the manual paper feed mode. Paper present at LOW.
⑬	Pick-up roller	Manual feed peper pick-up roller.
⑭	Paper feed roller	Manual paper feed roller (Includes the one-way clutc.)
⑮	Paper separation roller	The manual paper feed separation roller prevents agaist multi paper feed.
⑯	(PPD1) Paper transport sensor	Detects paper entry from the main body or the desk.

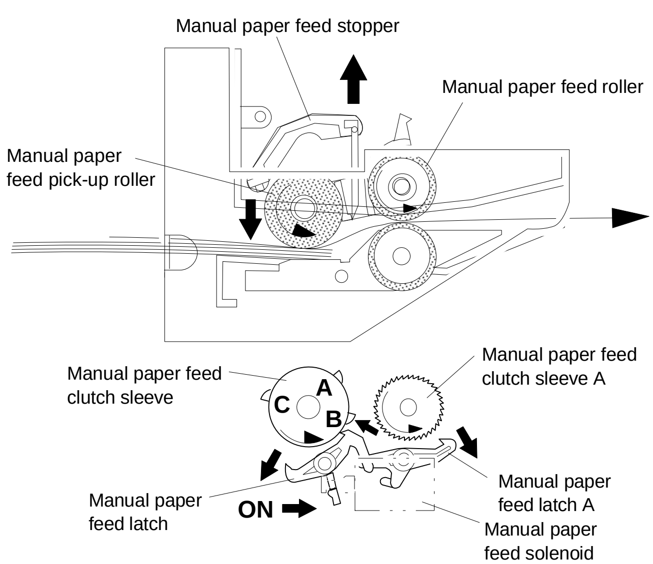
3. Basic operation

(1) Manual paper feed section operations

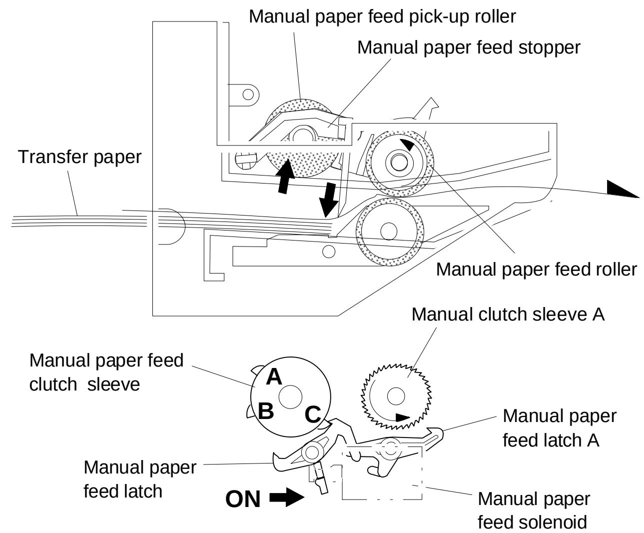
① Before the operation of the manual paper feed section, the manual paper feed solenoid (MPFS) is OFF and the manual paper feed stopper is closed and the paper pick-up roller is up. The latch and the clutch are at positions as shown in the table below.



② When the start button is pressed, the manual paper feed solenoid (MPFS) is turned on, and the manual paper feed latch A is disengaged from the manual paper feed clutch sleeve A, and the manual paper feed roller and the manual paper feed pick-up roller rotate. At the same time, the manual paper feed stopper is opened and the manual paper feed pick-up roller is pressed on the paper to start paper feed.

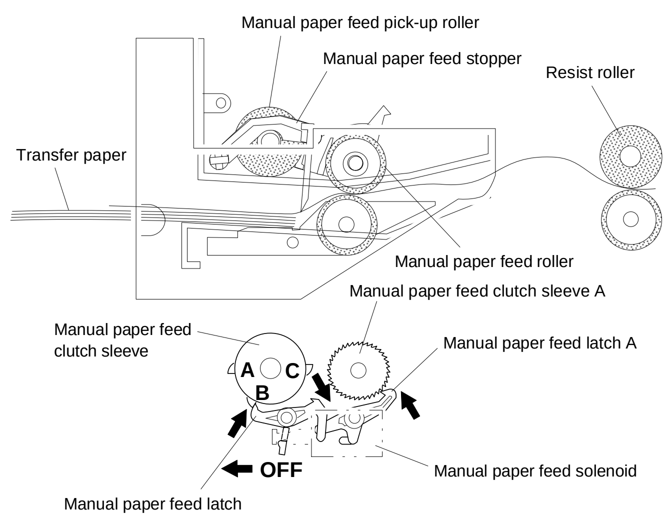


③ When the manual paper feed clutch sleeve pawl C is caught by the manual feed latch, the manual fed stopper falls and the manual feed pick-up roller rises. At the time, the transport roller is rotating.



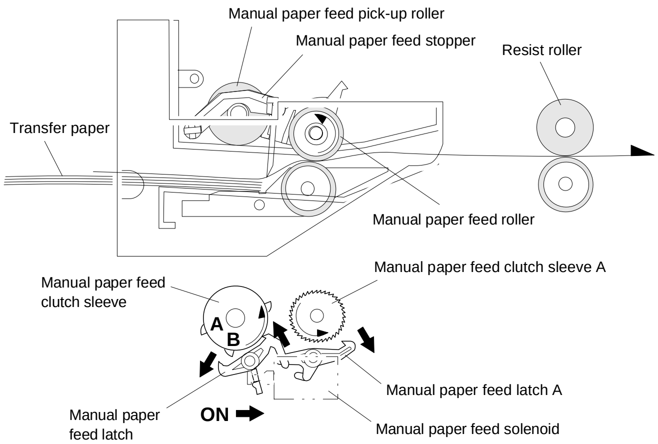
④ When the tip of the transferred paper is detected by PPD2, the manual paper feed solenoid is turned off after about 0.2 sec. At that time, the clatch sleeve pawl B is caught by the manual paper feed latch.

As a result, the paper is warped between the resist roller and the paper feed roller.

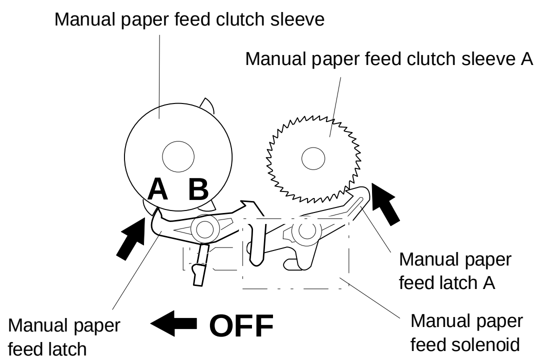


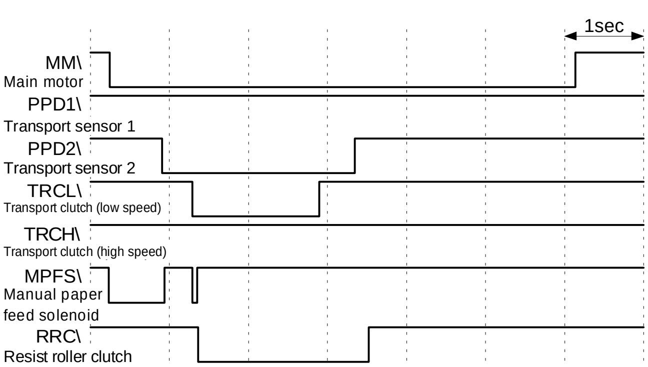
⑤ The manual paper feed solenoid is turned on for 0.08 sec in synchronization with rotation of the resist roller, and the manual peper feed roller is rotated. Therefore, paper jams due to insufficient pick-up of the resist roller is prevented.

At that time, the manual paper feed pick-up roller remains up.



⑥ The manual paper feed solenoid is turned off and the clutch sleeve pawl A is caught by the manual paper feed latch and the mamual paper feed is completed.





Manual paper feed timing chart

(2) Cassette paper feed section operations

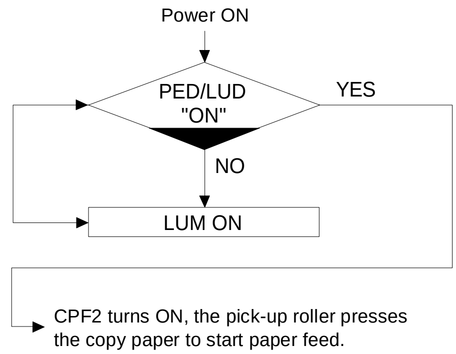
The cassette paper feed operations are the same in the paper tray 1 and the paper tray 2.

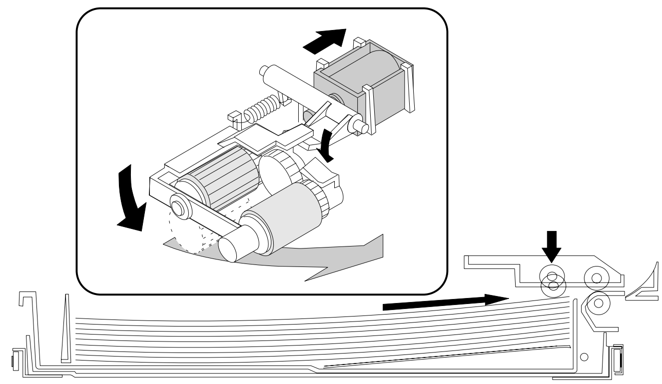
The following descriptions are based on the paper tray 1.

① Lift up

When the power is turned on, the main circuit checks the sensors.

The lift up motor is turned on/off to make ready for paper feed according to the states of the paper empty sensor (PED) and the lift-up senosr (LUD).





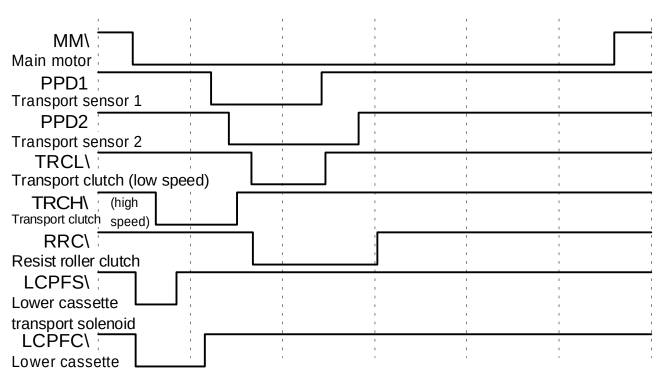
② Paper feed

When the start button is pressed, the cassette paper feed solenoid (CPFS2) and the cassette paper feed roller clutch (CPFC2) are turned on. By turning on the solenoid, the paper feed pick-up roller is pressed down to press the paper.

By turning on the clutch, the paper feed roller and the pick-up roller start the paper feed operation.

The fed paper is passed through the paper entry sensor (PID) to the transport roller.

the transport roller is rotated by two drive clutches. For transport from the paper feed section to the resist roller, It is driven by the high speed clutch. The resisted paper is transported to the process section in synchronization with the optical system. The transport speed at that time is switched from the high speed clutch to the low speed clutch so that the transport speed becomes the same as the process rotating speed.



Lower cassette paper feed timing chart

[5] TRANSPORT AND FUSING SECTIONS

1. Outline

The AR-5132 allows paper transport of max. A3 (11" × 17") to min. A5 (8 1/2" × 5 1/2").

After transfer of images, the paper is separated from the drum and transported to the fusing section by rotation of the resist roller and the transport belt.

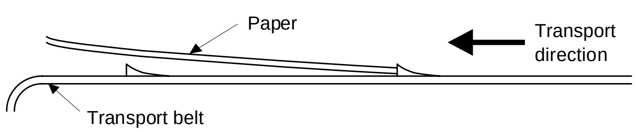
The transport section is provided with the separation sensor (PSD). This sensor detects separation of paper and is used for taking the drive timing of the duplex gate solenoid (DGS) after fusing.

2. Basic composition and functions

(1) Transport section

① Transport belts (2 pcs.)

The transport belts are corrugated to push the rear edge of paper.



② Separation sensor (PSD)

This is a transmission type photo sensor and is attached to the chassis of the main body.

③ Suction fan motor and ozone filter

Ozone generated in the process high voltage section is absorbed by the filter.

(2) Fusing section

① Upper heat roller

This roller is teflon-coated in the shape of a reversed crown.

② Lower heat roller

This roller is a silicon rubber roller in the shape of a crown.

③ Upper cleaning roller

This roller, impregnated with silicon oil, is used to remove dirt from the upper heat roller to provide better separation of paper and lengthens the life of the heat roller.

④ Separation pawl

Four separation pawls which are teflon-coated are used for the upper heat roller for reducing friction.

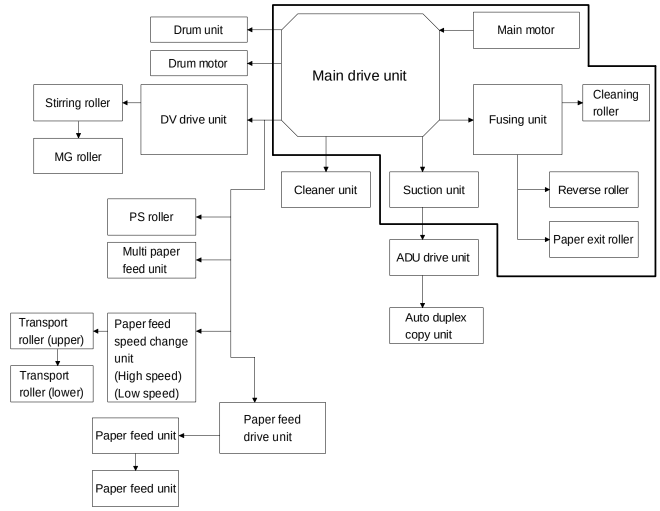
Two separation pawls are used for the lower heat roller.

⑤ Upper/lower separation function

The upper heat roller section and the lower heat roller section can be separated from each other for better serviceability.

⑥ Division of the drive system

The fusing unit is driven by the main drive unit. Since the fusing section is manually fed in case of a paper jam, a spring clutch is provided in the main drive gear to prevent that an excessive load is applied to the gears.



[6] HIGH VOLTAGE SECTION

1. Outline

There are three kinds of chargers; the main charger, the transfer charger, and the separation charger. The main charger employs the scorotron system. The drum surface is charged negatively and uniformly by electric charges controlled by the screen grid which is positioned between the charger and the drum.

The transfer charger is used to transfer toner images which are on the drum to the copy paper. A negative high voltage is applied to the back of the copy paper.

The separation charger applies AC corona to the copy paper to eliminate a potential difference between the drum in order to perform separation.

2. Basic composition

(1) Main charger high voltage transformer (MHVG)

	Grid voltage	Developing bias voltage
Standard mode	–490V	–400V
Photo mode	–490V	–400V
TSM mode	–440V	–350V
Printer mode	–460V	–400V

(2) Transfer charger high voltage transformer (THVG)

+13.5µA (Electrode sheet front/rear balance difference: within 3µA)

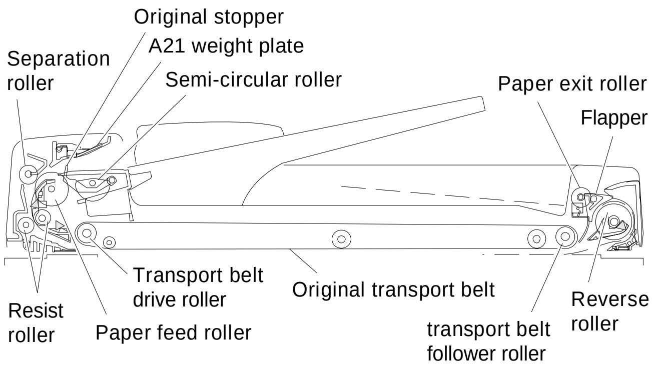
(3) Separation charger high voltage transformer (SHVG)

DC component voltage: –400±10V

[7] RADF MECHANISM SECTIONS

1. Operation flowchart

The figures below show the transport path of an document from the document setting, through paper feed, copying, to paper exit. For details of operations, refer to the operation process.



1) RAD mode (duplex copy mode) copying

START
↓
Step 01: The transport section is closed. (AUOD ON)
↓
Step 02: An document is set on the document tray. (DSS output HIGH)
↓
Step 03: Document feed display ON
↓
Step 04: Print SW ON
↓
(Preliminary paper feed): ∗ A: For the first document, dummy paper exit is performed.
↓
∗ A Step 05: Paper feed motor (DFM) forward rotation (Paper feed roller, semi-circular roller rotation) Since the stopper is up, paper feed is not performed.
↓
Step 06: Reverse motor (DRM) forward rotation (Reverse roller, paper exit roller rotation)
↓
Step 07: Transport motor (DTM) rotation (Transport belt rotation)
∗ B: If there has been an document on the tray, is discharged.
↓
∗ A Step 08: Paper feed motor (DFM) OFF
Paper feed solenoid (DFSOL) ON
(The weight plate and the stopper move down to press the document onto the semi-circular roller.)
↓
Step 09: Paper feed motor (DFM) forward rotation (Paper feed roller, semi-circular roller rotation)
The document feed is started.
↓
∗ B Step 10: Reverse sensor (RDD) senses the lead edge of the discharged document. (RDD output HIGH)
↓
Step 11: Document feed sensor (DFD) senses the lead edge of the discharged document. (DFD output HIGH)
↓
Step 12: Paper feed motor (DFM) OFF
The document is stopped by the resist roller.
↓
Step 13: Paper feed motor (DFM) reverse rotation (Resist roller rotation)
The lead edge of the document is taken up by the resist roller.)
↓
Step 14: Document width sensor (DWS) senses the document width. (Output LOW)
↓
Step 15: Document timing sensor (DTD) senses the lead edge of the document. (DTD output HIGH)
↓
Step 16: Paper feed motor (DFM) OFF
(The document is stopped with its lead edge taken up by the resist roller.)
↓
∗ B Step 17: Reverse sensor (RDD) senses the rear edge of the discharged document. (RDD output LOW)
Reverse motor (DRM) rpm down
↓
Step 18: Transport motor (DTM) OFF
(Transport stop)
↓
∗ B Step 19: Document discharge
↓
Step 20: Reverse motor (DRM) OFF
(Reverse roller, paper exit roller stop)
(Paper feed reverse)
↓
(Preliminary paper feed):
↓
Step 21: Transport motor (DTM) forward rotation
Transport motor, reverse motor (DRM) forward rotation (Reverse roller, paper exit roller rotation)
↓
Step 22: Paper feed motor (DFM) reverse rotation (Resist roller rotation)
The document is sent to the transport section.
↓
Step 23: Document feed sensor (DFD)
Senses the rear edge of the discharged document. (DFD output LOW)
↓

∗ C Step 24: Paper feed solenoid (DFSOL) OFF
(The weight plate and the stopper move up.)

∗ C: If there is no document on the document tray, move up the stopper and the weight plate.

↓

Step 25: Document width sensor (DWS) output HIGH

↓

Step 26: Document timing sensor (DTD) senses the rear edge of the document.
(DTD output LOW)
Paper feed motor (DFM) OFF (Resist roller stop)
Reverse solenoid (DRSOL) ON (The flapper move up.)

↓

Step 27: Reverse sensor (RDD) senses the lead edge of the document. (RDD output HIGH)

↓

Step 28: The lead edge of the document is moved counterclockwise by the flapper.

↓

Step 29: Transport motor (DTM) OFF
(Transport belt stop)

↓

Step 30: Reverse motor (RDM) OFF
(Reverse roller, paper exit roller stop)

↓

Step 31: Transport motor (DTM) OFF
(Transport belt rotation)

↓

Step 32: Reverse motor (DRM) forward rotation
(Reverse roller, paper exit roller rotation)
The document is transported to the paper feed section.

↓

Step 33: Paper exit sensor (RDD) senses the rear edge of the reverse document.
(RDD output LOW)

↓

Step 34: Reverse motor (DRM) OFF
(Reverse roller, paper exit roller stop)

↓

Step 35: Transport motor (DTM) OFF
(Transport belt stop)
Document stop

↓

Step 36: Reverse solenoid (DRSOL) OFF
(The flapper moves down.)

↓

Step 37: Copier mirror base scanning is started.

∗ D ↓

DSS output — LOW (There is no document on the tray.) → After completion of mirror base scanning, go to step 64. (Reverse rotation)

HIGH (There is an document on the tray)

↓

(Preliminary paper feed)

↓

Step 38: Paper feed motor (DFM) forward rotation
(Paper feed roller, semi-circular roller rotation)
The document feed is started.

↓

Step 39: Document feed sensor (DFD) senses the lead edge of the document.
(DFD output HIGH)

↓

Step 40: Paper feed motor (DFM) OFF
The document is stopped by the resist roller.

↓

Step 41: Paper feed motor (DFM) forward rotation
(Resist roller rotation)
The lead edge of the document is taken up by the resist roller.

↓

Step 42: Document width sensor (DWS) senses the document width. (Output LOW)

↓

Step 43: Document timing sensor (DTD) senses the lead edge of the document. (DTD output HIGH)

↓

Step 44: Paper feed motor (DFM) OFF
(The document is stopped with its lead edge taken up by the resist roller.)

↓

Step 45: Copier mirror base scanning stop

↓

(Reverse rotation)

↓

Step 46: Reverse solenoid (DRSOL) ON
(The flapper moves up.)

↓

Step 47: Transport motor (DTM) forward rotation
(Transport motor rotation)
Reverse motor (DRM) forward rotation
(Rreverse roller, paper exit roller rotation)

↓

Step 48: Reverse sensor (RDD) senses the lead edge of the document.
(RDD output HIGH)

↓

Step 49: The lead edge of the document is moved counterclockwise by the flapper.

↓

Step 50: Transport motor (DTM) OFF
(Transport belt stop)

↓

Step 51: Reverse motor (DRM) OFF
(Reverse roller, paper exit roller stop)

↓

Step 52: Transport motor (DRM) reverse rotation
(Transport belt rotation)

↓

Step 53: Reverse motor (DRM) reverse rotation (Reverse roller, paper exit roller rotation) The document is transported to the paper feed section.

↓

Step 54: Reverse sensor (RDD) senses the rear edge of the reversed document. (RDD output LOW)

↓

Step 55: Reverse motor (DRM) OFF (Reverse roller, paper exit roller stop)

↓

Step 56: Transport motor (DTM) OFF (Transport belt stop) Document stop

↓

Step 57: Reverse solenoid (DRSOL) OFF (The flapper moves down)

↓

Step 58: Copier mirror base scanning start

↓

Step 59: Copier mirror base scanning stop

∗ E ↓

First-out document — NONE → After completion of mirror base scanning, go to step 82.

YES ↓

(Paper exit paper feed reverse)

↓

Step 60: Transport motor (DTM) forward rotation (Transport belt rotation) Reverse motor (DRM) forward rotation Reverse roller, paper exit roller rotation) The document is discharged.

↓

Step 61: Paper feed motor (DFM) reverse rotation (Resist roller rotation) The document is sent to the transport section.

↓

Step 62: Document feed sensor (DFD) senses the rear edge of the document. (DFD output LOW)

↓

∗ C Step 63: Paper feed solenoid (DFSOL) OFF (The weight plate and the stopper moves up.)

∗ C: When there is no document on the tray, move up the stopper and the weight plate.

↓

Step 64: Document width sensor (DWS) output LOW

↓

Step 65: Document timing sensor (DTD) senses the rear edge of the document. (DTD output LOW)

↓

Step 66: Reverse sensor (RDD) senses the lead edge of the discharged document. (RDD output HIGH)

↓

Step 67: Transport motor (DTM) rpm down

↓

Step 68: Document discharge

↓

Step 69: Reverse solenoid (DRSOL) ON (The flapper moves up.)

↓

Step 70: Transport motor (DTM) forward rotation (Transport belt rotation) Reverse motor (DRM) forward rotation (Reverse roller, paper exit roller rotation)

↓

Step 71: Reverse sensor (RDD) senses the lead edge of the document. (RDD) output HIGH)

↓

Step 72: The lead edge of the document is moved counterclockwise by the flapper.

↓

Step 73: Transport motor (DTM) OFF (Transport belt stop)

↓

Step 74: Reverse motor (DRM) OFF (Reverse roller, paper exit roller stop)

↓

Step 75: Transport motor (DTM) reverse rotation (Transport belt rotation)

↓

Step 76: Reverse motor (DRM) forward rotation (Reverse roller, paper exit roller stop) The document is sent to the paper feed section.

↓

Step 77: Reverse sensor (RDD) senses the rear edge of the reverse document. (RDD output LOW)

↓

Step 78: Reverse motor (RDD) senses the rear edge of the reversed document. (RDD output LOW)

↓

Step 79: Transport motor (DTM) off (Transport belt stop) Document stop

↓

Step 80: Reverse solenoid (DRSOL) OFF (The flapper moves down.)

↓

Step 81: Copier mirror base scanning start

∗ D ↓

DSS output — LOW (No document on the tray) → After completion of mirror base scanning, go to step 46 (reverse).

HIGH (There is an document on the tray.) → Go to step 38 (Preliminary paper feed).

↓

(Paper exit)

↓

Step 82: Transport motor (DTM) forward rotation
(Transport belt rotation)
Reverse motor (DRM) forward rotation
(Reverse roller, paper exit roller rotation)
The document is discharged.

↓

Step 83: Reverse sensor (RDD) senses the lead edge of the discharged document.
(RDD output HIGH)

↓

Step 84: Reverse sensor (RDD) senses the rear edge of the discharged document.
(RDD output LOW)
Transport motor (DTM) OFF
(Transport belt stop)
Reverse motor (DRM) rpm down

↓

Step 85: Document discharge

↓

Step 86: Reverse motor (DRM) OFF
(Reverse roller, paper exit roller stop)

↓

END

Note: ∗ A: For the first document, the preliminary paper feed operation is performed.

∗ B: When there is an document on the document tray in advance, it is discharged.

∗ C: When there is no document on the document tray, move up the weight plate and the stopper.

∗ D: When there is no document on the document tray, the document set sensor (DSS) output becomes LOW.

∗ E: It depends on whether there is any preliminary fed document in step 38 ~ step 44.

2. Document size detection

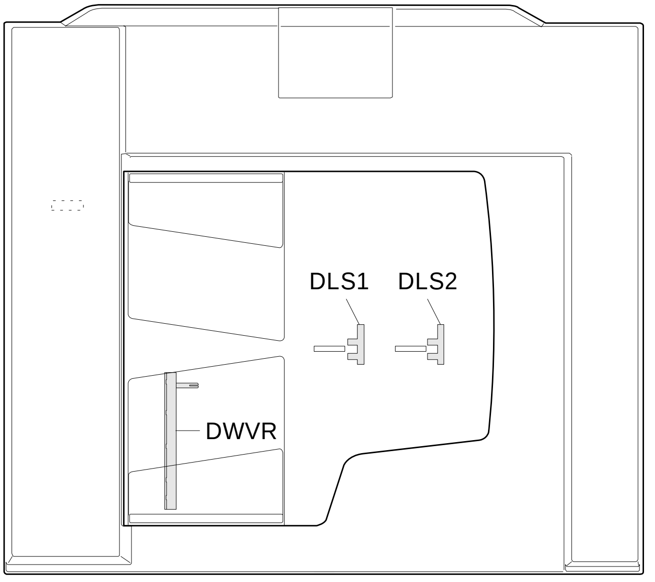
The document size is detected in three ways of different purposes.

1) Document size detection by the document set tray

The document size detection by the document set tray is used in automatic paper size and automatic magnification selection mode, in order to recognize the document size when the document is set on the document tray, allowing the automatic selection of paper size and magnification ratio of copy.

When documents composed of sheets of different sizes are set, this detection method recognizes the largest sheet as the document size, which is determined by the width measured by the document width volume (DWVR) and the length measured by the document length sensors (DLS1, DLS2).

The document size is determined in the timing of document sensing by the document set sensor (DSS).



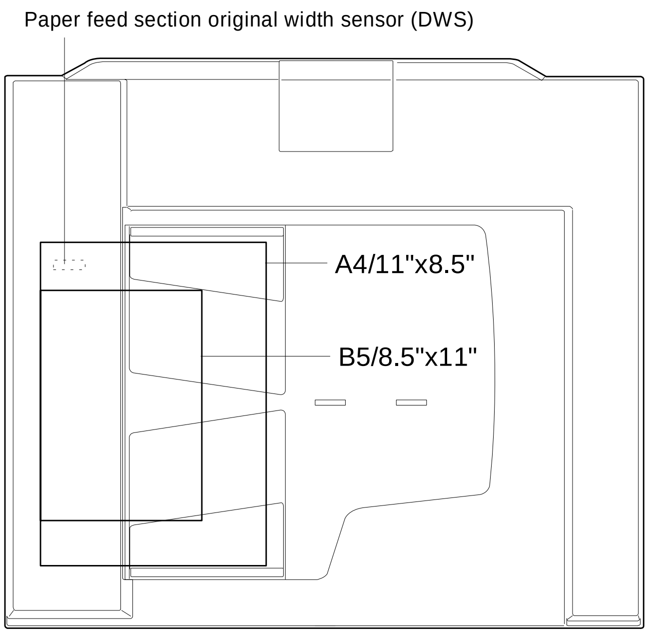
	Document size, setting orientation	○: ON or L output (sensed) ●: OFF or H output		
		DWVR	DLS1	DLS2
AB series	A4	3	●	—
	B5	4	●	—
	A5	5	●	—
	A5R	7	●	—
	B5R	6	○	—
	A4R	5	○	—
	B4	4	○	—
	A3	3	○	—
Inch series	11" × 8.5"	0	●	●
	8.5" × 5.5"	1	●	●
	8.5" × 5.5"R	2	●	●
	11" × 8.5R"	1	○	●
	14" × 8.5"	1	○	○
	11" × 17"	0	○	○

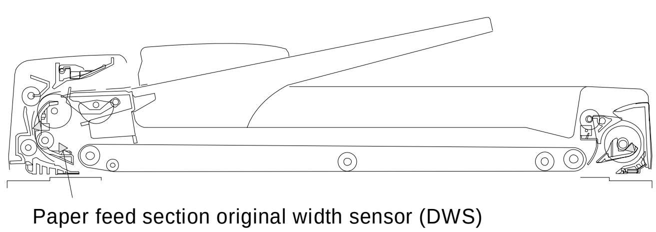
2) Document size detection by the document width sensor (DWS) in the paper feed section

The document size detection by the document width sensor (DWS) in the paper feed section is used in automatic paper size and automatic magnification ratio selection mode to determine whether the document is A4 or A5 (11" x 8.5" or 8.5" x 5.5").

When documents composed of stacked sheets of different sizes are set in the document tray, the document size cannot be detected by the sensors in the document tray. Therefore, this function is provided to sense the document size behind the resist roller after the paper feed section has fed the document, as far as documents of A4 or A5 size (11" x 8.5" or 8.5" x 5.5") (portrait) is concerned. Consequently, if A4- and A5-size (11" x 8.5" or 8.5" x 5.5") documents (portrait) are stacked and set in the document tray, the document size detection by the paper feed section document width sensor (DWS) has the priority over the document size detection by the document set tray.

When A4- and A5-size (11" x 8.5" and 8.5" x 5.5") documents (portrait) are stacked and set in the document tray, the document length sensors (DSL1, DSL2) are not actuated. Therefore, the document width is sensed by the paper feed section document width sensor (DWS) to judge A4 or A5 (11" x 8.5" or 8.5" x 5.5").





Paper feed section document width sensor (DWS) status

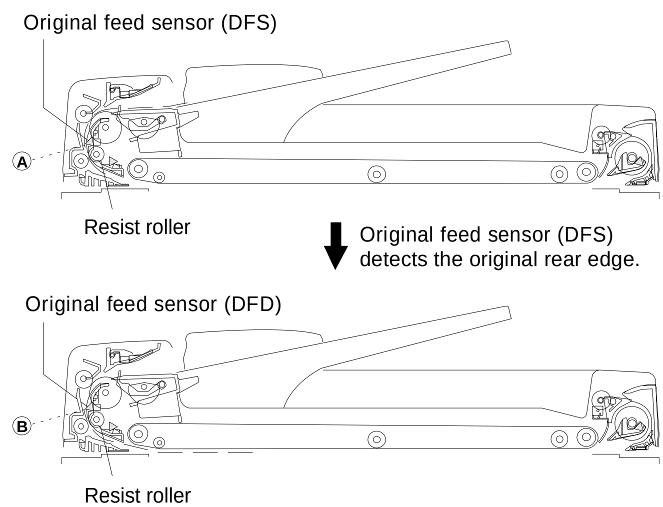
Document size	○: Output LOW (Detection) ●: Output HIGH
A4/11″ × 8.5″	○
B5/8.5″ × 11″	●

3) Document size detection by the paper feed motor rotation sensor (DFMRS)

This function compensates for the inaccuracy of the document size recognition in the document tray when documents of different sizes are stacked in the document tray. That is, results of this function has priority over the document size detection in the document tray. The pulses of the slit disc rotation of the feed motor (DFM) are counted in the period before the rear edge of document is sensed (DFD output LOW) by the document feed sensor after the feed motor (DFM) has started reverse rotation, that is, after the resist roller has started rotating and feeding of document from the fed section to the transport section has been started, to determine the document length.

To improve detection accuracy, the document width is sensed also by the paper feed section document width sensor (DWS).

Resist roller rotation start (The document is fed from the paper feed section.)



The paper feed motor rotation sensor (DFMRS) counts the number of rotations of the paper feed motor (DFM) between Ⓐ and Ⓑ to judge the document length.

[8] DESK UNIT MECHANISM SECTION

1. Operation flow chart

A. Paper tray 2 (Normal copy mode)

Paper feed start <Copier print switch ON>

↓

STEP 01: JOB command start command reception
- Transport motor ON

↓

STEP 02: Paper feed request reception (Preliminary paper feed command or paper feed command)
- Pickup solenoid ON
- Transport select clutch ON

↓

STEP 03: Resist sensor 1 (upper) ON
- Timer A start
  Pickup solenoid OFF, resist transport clutch ON
- Timer B start
  For sending the preliminary paper feed end command
- Timer C start (according to paper size)
  Transport select clutch OFF timer

↓

STEP 04: Timer A up
- Pickup solenoid OFF
- Resist transport clutch OFF

↓

STEP 05: Timer B up
- Preliminary paper feed end command sending

↓

Preliminary paper feed command — NO → To STEP 08

YES ↓

STEP 06:
- Timer C temporal stop
- Transport select clutch OFF
- Resist transport clutch OFF

↓

Paper feed command signal wait

RECEPTION → To STEP 20

↓

STEP 07
- Timer C restart
- Transport select clutch ON
- Resist transport clutch ON

↓

STEP 08:

↓

STEP 09: Timer C up
- Transport select clutch OFF

↓

STEP 10: Resist sensor 1 (Upper) OFF
- Paper feed end command sending
- Resist transport clutch OFF timer start

↓

STEP 11:

↓

STEP 12: Resist transport clutch OFF, timer up
- Resist transport clutch OFF

↓

JOB command reception — NO → To STEP 02

YES ↓

STEP 13: Paper feed operation end
- Transport motor OFF

STEP 20: After reception of the paper feed command, the main body transport clutch (trc signal) is monitored in parallel with operations of STEP 07 or later.

↓

STEP 21: Copier transport clutch (trc signal) OFF confirming

↓

STEP 22: Copier transport clutch (trc signal) ON confirming

↓

STEP 23: Copier transport clutch (trc signal) OFF confirming
- Resist transport clutch OFF

B. Paper tray 3

Paper feed start <Copier print switch ON>

↓

STEP 01: JOB command start command reception
- Transport motor ON

↓

STEP 02: Paper feed request reception (Preliminary paper feed command or paper feed command)
- Separation clutch ON

↓

STEP 03: Resist sensor 2 (lower) ON
- Resist loop pulse set

↓

STEP 04: Resist loop pulse up
- Resist transport clutch ON
- Pulse set for the separation clutch OFF
- The next paper is prepared in the desk. (Shift from collect section 2 → collect section 1)

↓

STEP 05: Separation clutch OFF, pulse up
- Separation clutch OFF

↓

STEP 06: Resist sensor 1 (upper) ON
- Pulse set for the preliminary paper feed position stop

↓

STEP 07: Preliminary paper feed position stop, pulse up
- Resist transport clutch OFF
- Transport speed: Speed reduction start (380mm/s → 295mm/s)
- Preliminary paper feed end command sending timer start

↓

STEP 08: Preliminary paper feed end command sending, timer up
- Preliminary paper feed end command sending

↓

Preliminary paper feed end command? — NO → To STEP 09

↓ YES

Paper feed command reception wait

↓ RECEPTION

STEP 09:
- Resist transport clutch ON

↓

STEP 10: Resist sensor 1 (upper) OFF
- Paper feed command sending timer start

↓

STEP 11: Paper feed command sending, timer up
- Paper feed end command sending
- Resist transport clutch OFF
- Transport clutch: Acceleration start (295mm/s → 380mm/s)

↓

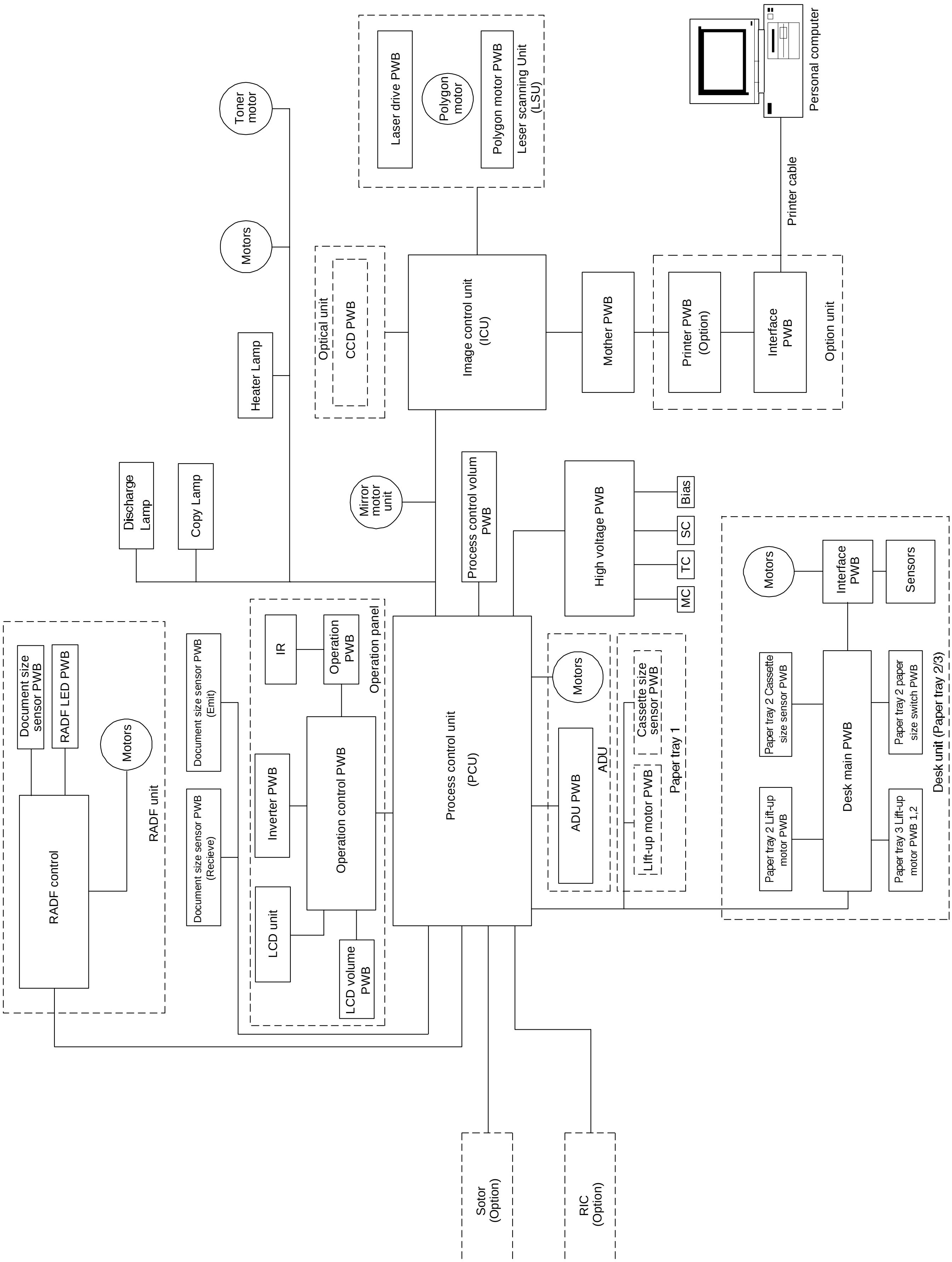
JOB end command reception? — NO → To STEP 02

↓ YES

STEP 12: Paper feed operation end
- Paper feed motor OFF

[9] ELECTRICAL SECTION

1. Block diagram



2. ICU PWB

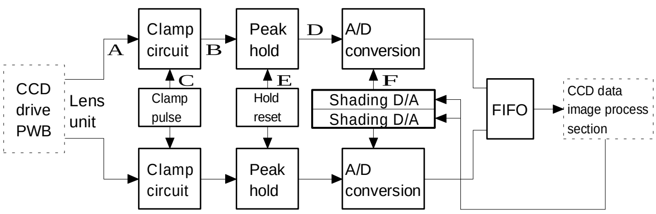
(1) CCD control section

Basic functions

① Generation of the timing signal to the lens unit CCD drive PWB.

② Process of the analog signal from the lens unit CCD drive PWB, and the A/D converting section.

③ Shading correction/signal control process



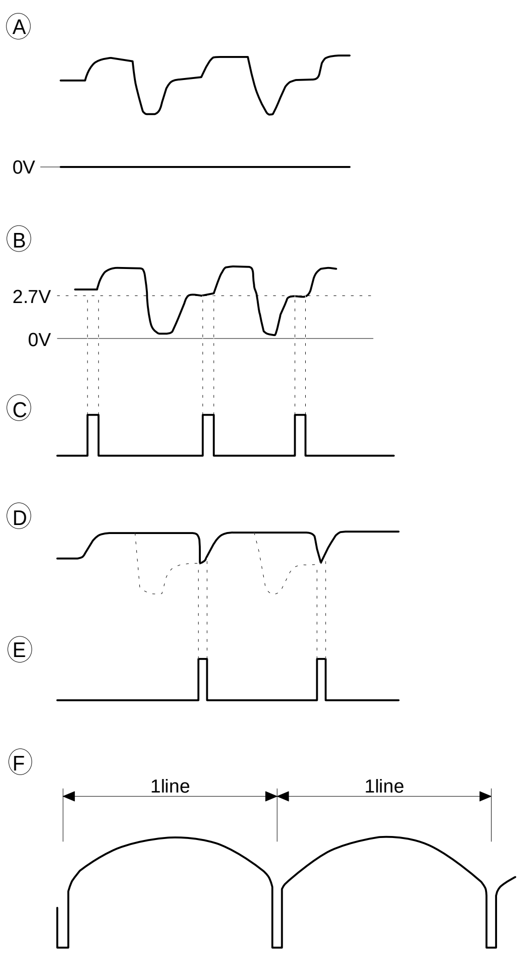
Operational description

The CCD image signal output pins of two system (ODD, EVEN) for one line to allow high-speed process.

The output signals from the output pins are separately processed in defferent circuits as described below before being sent to the PCU.

The impedance of the CCD signal Ⓐ amplified by the CCD drive PWB (lens unit) is converted and sent to the clamp circuit, where the black level is clamped to 2.7V at the timing of the CLMP signal Ⓒ by the analog switch Ⓑ.

The analog signal Ⓓ which was clamped is sent to the FIFO memory after AD conversion. The peak hold is reset by the VRST signal Ⓔ for every pixel.



In the A/D conversion, by turning off the shading correction data, the CCD element fluctuation and the optical system (lamp, lens) light quantity fluctuation are corrected, and the analog data are converted into 8-bit digital data between the white level and the black level.

The 8-bit image data converted in the even and the odd circuits are stored in FIFS by one pixel at one time alternately.

These data are taken out sequentially to output the image data of one array to the image process section.

5150 pixel CCD linear sensor (Monochrome)

(Outline)

The ILX510 is two-output system reduction type CCD linear sensor, which scans an A3 Document in 400 dpi.

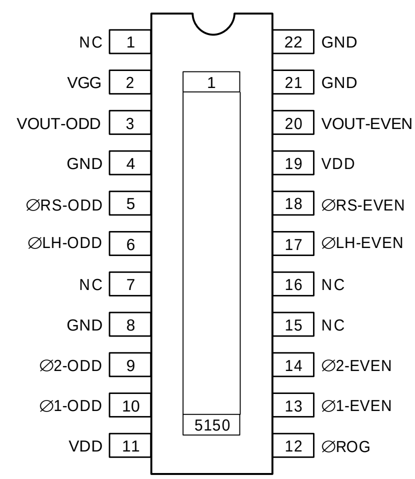
(Features)

- Number of effective pixels: 5150 pixels
- Pixel size: 7 µm × 7 µm (7 µm pitch)
- Max. data rate: 40MHz
- Power voltage: 12V U1 battery
- All input clocks: CMOS 5V drive

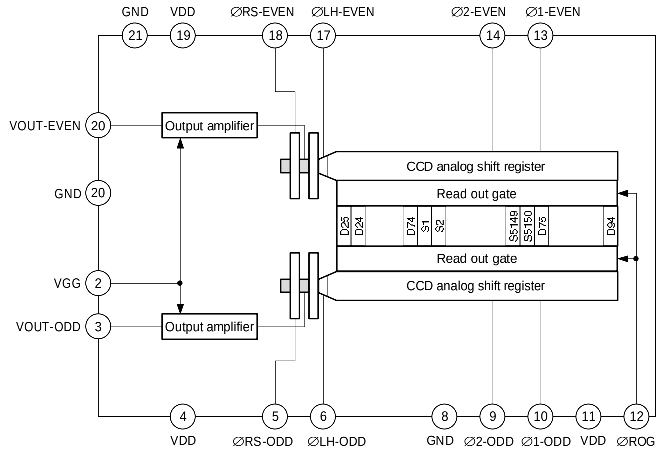
(Absolute max. rating)

- Power voltage: VDD 15V

Pin arrangement (Top view)



Block diagram



CCD GA pin index

Pin No.	Pin name	Function
1	NC	
2 ≀ 8	AD0 ≀ AD6	Odd number pixel A/D conversion result
9	AD7	Odd number pixel A/D conversion result
11	BD0	Odd number pixel A/D conversion result
12 ≀ 18	BD1 ≀ BD7	Odd number pixel A/D conversion result
20	BD8	Sync signal from LSU (HSYNC)
21	SMODE	Self running mode selection (in the shading correction)
22	WB	Shading writing white/black control
23	SHINHB	Shading effective signal
24	RESB	Reset signal
25	ADRSTB	In shading black writing, initialize at 0. Address reset black
28	WRCK	Shading writing clock
30	32MCK	32MHz input
32	TST	GA test pin
33	DACKE	Even number D/A clock
34	DACK0	Odd number D/A clock
35	CCDCK	Clock to be sent to the CCD PWB
36	ROGB	ϕ ROG signal to be sent to the CCD PWB
37	SETB	Sent to the CCD PWB to make ϕ LH signal valid. Valid at 1.
38	CLMP	Clamp signal
39	VRST	Capacitor discharge signal
40	ADCK	A/D clock
41	FWCK	Write clock to the FIFO for image output
42	8MCK	8MHz clock
44	PXCK	Image output pixel clock
45	RRESB	Image output FIFO /RSTR (read reset)
46	RREB	Image output FIFO /RE (read enable)
47	SRCK	White correction data read clock
48	SRRESB	White correction data FIFO /RSTR (read reset)
49	SRREB	White correction data FIFO /RE (read enable)
50	SWCK	White correction data FIFO WCK (write clock)
51	SH	Line sync signal
53 ≀ 61	ABD0 ≀ ABD7	Odd number/even number synthesized pixel signal
63	BWCKE	Black correction data write clock (even number)
64	BWCK0	Black correction data write clock (odd number)

[CCD GA and peripheral circuit]

The CCD control GA and the peripheral circuit are connected as shown in the figure on the next page.

[CCD GA functions]

The CCD GA functions are classified as follows:

A. CCD reading

B. Shading correction data writing

The CCD reading is further classified as follows:

a. Supply of clocks and timing signals to the CCD PWB (which includes the CCD)

b. Supply of timing signals to the analog circuit which processes the output signal from the CCD PWB

c. Supply of timing signals to the A/D convertor, the D/A convertor, and the digital circuits.

There are following kinds of digital circuit.

- FIFO for shading (for white correction)
- Latch for shading (for black correction)
- FIFO for output of image data

d. Image data of the odd number channel and the even number channel which are A/D converted are synthesized into one line.

The CCD reading operation is divided into the dependent running mode and the self running mode by setting of the SMODE pin.

The dependent running mode is for copiers. Reading of one line is performed at falling of the HSYNC signal from the LSU. Then the machine enters the standby state for the next falling of the HSYNC signal.

Therefore reading of one line is always synchronized with falling of the HSYNC signal.

If the HSYNC interval falls below the specified level (326.5µs), the HSYNC is dropped.

Since reading of one line is based on the counter operating at 8MHz inside the GA, an error of max. 125ns is generated from falling of the HSYNC to starting reading the one line.

When receiving image data through ICU, the SH which is outputted from the CCD GA is used as the reference of timing.

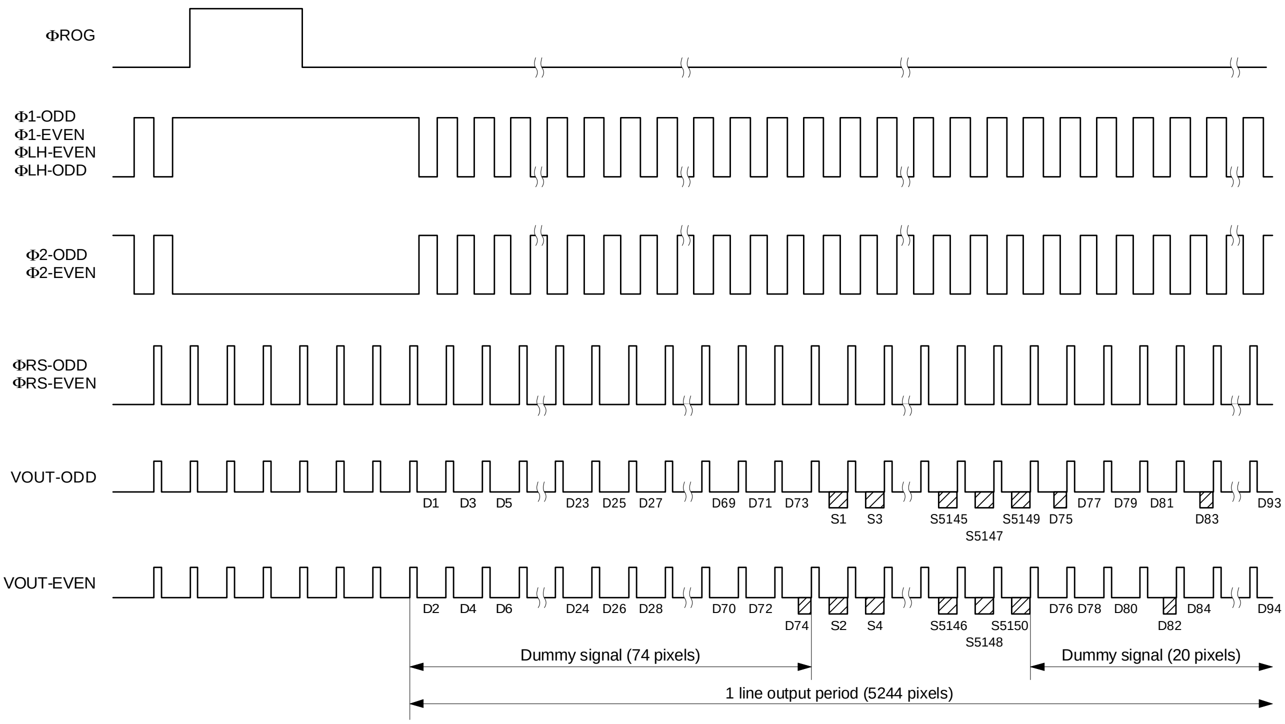
In the self running mode, reading is started regardless of the SYNC signal from outside when in shading correction.

Since reading of one line is started at the timing when the internal counter becomes zero, the counter itself becomes zero when reset is performed. Since the reset pin of the CCD control PWB is fixed to HIGH, the timing for starting reading the line depends on the initial state of the internal counter. The time (accumulated time, 334.38µs) for one line is 2675 counts in 8MHz in the self running mode.

The accumulated time in the dependent running mode is 334.21µs ±0.1% (the LSU specification). In the self running mode, therefore, the accumulated time is +0.05% of the standard value in the dependent running mode.

In either mode of the self running and the dependent running, the SH is used as the starting reference by the ICU, etc. The SH is turned HIGH for one frequency of the timing clock PKCK for sending image data from the CCD to the ICU.

<Timing chart>



[Image data reading]

The ILX510 has 5150 effective pixels.

In the CCD control section, the FIFO of 5048 pixels is provided for image data output and shading correction data, and 102 pixels out of it must be discarded.

Therefore, S49 ~ S5095 out of S1 ~ S5150 are enabled to output.

[Shading correction]

Corrections of light/dark areas are performed by changing the upper side and the lower side of the A/D reference voltage.

Setting of the reference voltage is performed by the D/C convertor built in 2Ch.

Since the light area correction is made for each pixel, the 8-bit correction data written into the FIFO are D/A converted to change the voltage at REF+ pin of the A/D convertor.

Two A/D convertors and two D/A convertors are provided for odd number pixels and even number pixels respectively, and they are operated at 8MHz.

Since there is only one FIFO, reading is made at 16MHz.

The dark area is divided into the odd number pixels and the even number pixels to change the voltage at REF- pin of the A/D convertor.

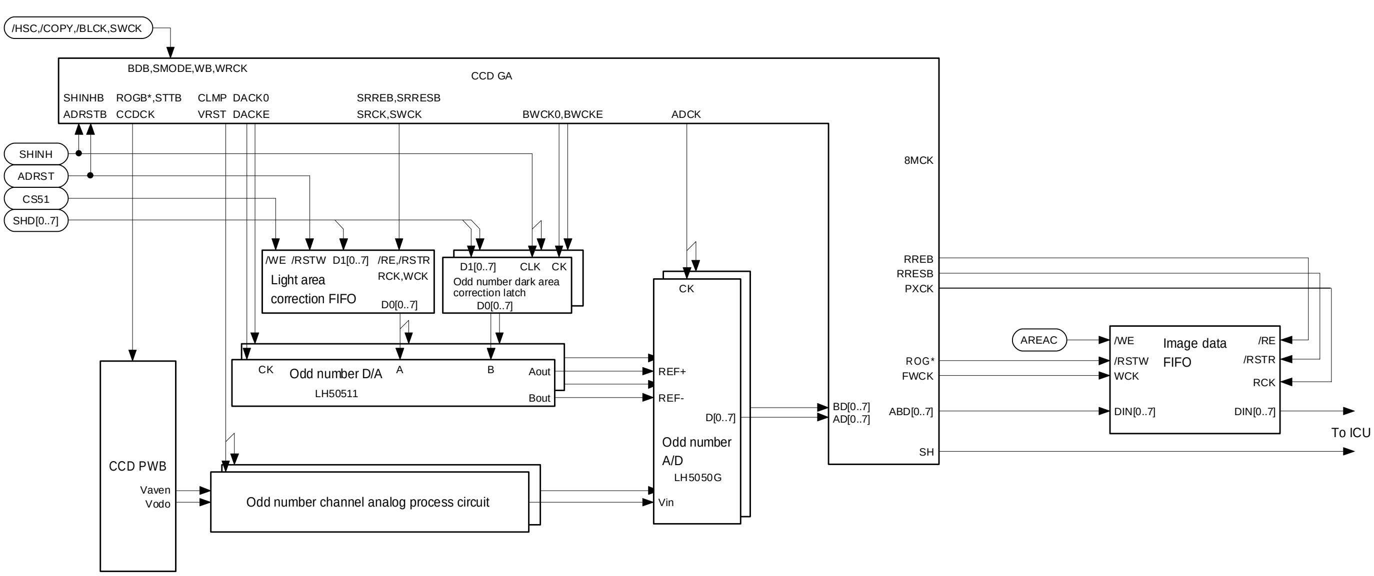
Two 8-bit latches (74AC273) are provided for the odd numbers and the even numbers. The value is D/A converted to set the voltage at REF- pin.

The output of the D/A convertor is a current output, which is converted into a voltage by the resistor and the transistor to input to the REF pin of the A/D convertor. The voltage supplied to the REF pin is slightly off-set by the ON voltage of the transistor even though the read value of the A/D convertor is directly set to the D/A convertor. Therefore correction must be performed from the read value in the shading correction.

IN the case of data reading for shading correction, the SHINH signal is driven LOW in order to maximize the light area and minimize the dark area.

By driving the SINH signal LOW, the dark area FIFO output is HIGH-Z, and the dark area latch is cleared.

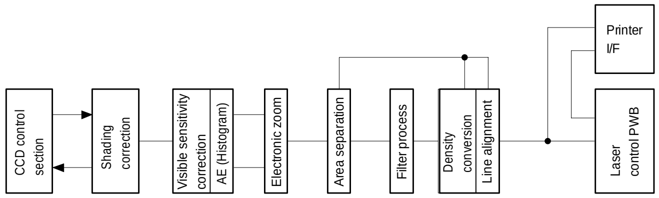
Since the FIFO output is pulled up, FFh and 00h are provided to the D/A convertor.



(2) Image process section

The image process section is composed of gate array A and gate array B, the SRAM for peripheral table, and the FIFO.

The image signal flow is shown as follows.

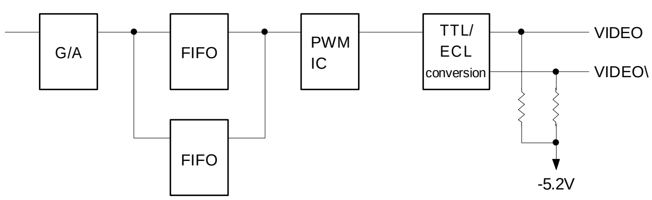


The image signals which was A/D converted according to the shading data from the image process section are converted into data which were subjected to the visible sensitivity (inverse function) correction and the auto exposure process. If the zooming mode is selected, electronic zooming is performed. Zooming in the sub scanning direction in this machine is performed by changing the moving speed of the optical system. In the main scanning direction, image data are electronically interpolated for zooming. Then the data are divided into the photo area, the hatched area, the character area, and the other area by the characteristics amount of the converted data and the peripheral pixels.

After that, the density conversion is performed to obtain the suitable density for each mode.

If the density conversion mode is the photo mode, lines are aligned to provide higher gradation before sending to the laser control section.

(3) Laser control section



Basic function

① Image digital signal → Laser drive PWM signal exchange

② PWM calibration control on starting printing

③ TTL → ECL conversion

④ Lim FIFO R/W control

Operational description

Image signals processed in the image process section are stored in the FIFO as the line image signals and inputted to the LCU G/A. The first print position signal (BD signal) from the LSU and the CKX4 are synchronized to align the image line positions. The line data are read from the FIFO and converted into the PWM width corresponding to the data by the IC and delivered to the LSU unit at the ECL level.

The LCU G/A takes the following four states with the PLAY, the LDON, and the image data signal to control the timing of laser control.

Laser state	LDONB	PLAYB	Image data
Stop	1	1	×
Forcibly ON	0	×	×
Image write	1	0	Image data
Void formation	1	0	White data

The LDONB signal forcibly turns on laser. It is driven LOW when the rotation ready signal of the polygon motor is sensed. Since the laser power is automatically performed by the LDONB, the LDONB requires LOW signal of 10ms or more. When the LDONB is LOW, the PLAYB signal is driven LOW to allow the LSU to operate.

[LSU GA and peripheral circuit]

The LSU GA functions are classified as follows.

- Control to write image data from the ICU to two FIFO's alternatively for every line.

  Input: GCK

  Output: F1WB, F2WB, FWCK, RSTWB

  (Image data themselves from the ICU are supplied to the FIFO directly.)

- Control to read image data from the FIFO to which data are not written.

  Output: F1RB, F2RB, FRCK, RSTRB, DIM [0..7]

- Generates the sync signal (BDB) for image clock and the ICU in synchronization with the sync signal (/SYNC) from the LSU.

  Input: CKX4, HSB

  Output: CLK, BDB

- According to instructions from the ICU, etc., control of the effective area in the main scanning direction and forcibly turning on the laser are performed.

  Input: SLAT, LSCK, LSIN, LDCNB, PALYB, CAL0

  Output: D0 [0..7]

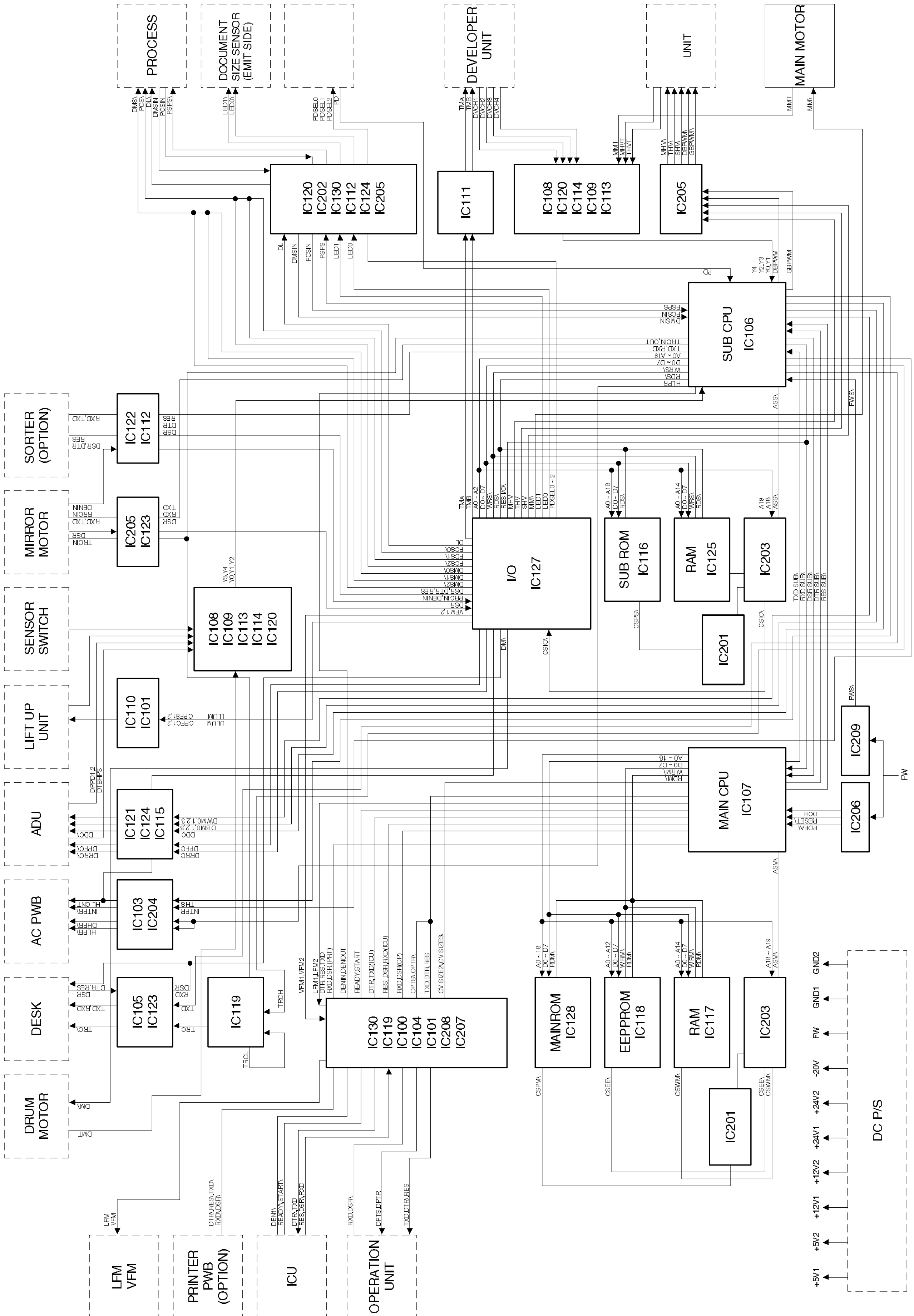
- PWM ICU calibration is performed at the start of turning on the laser.

  Input: LDBON, PLAYB, CAL0

  Output: CALIN

3. PCU PWB

(1) Block diagram (PCU PWB)



(2) Main CPU (IC107: H8/570)

① Outline

The CPU controls the loads in the body and sends and receives data to and from the various optional controllers through the serial data communication line and controls the system.

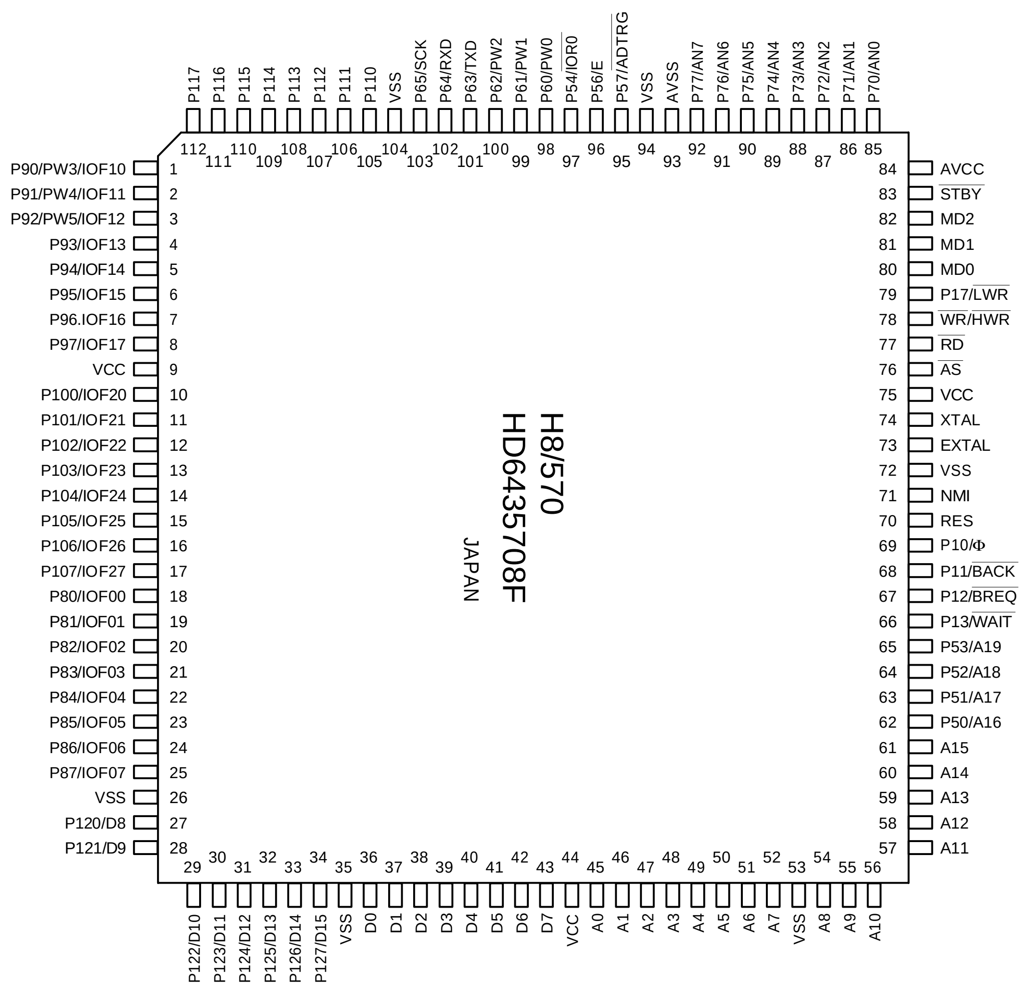
② Features

The H8/570 (CPU) is a single-chip microprocessor which performs the exclusively-used commands at high speeds to strengthen the routine operations such as the timer functions and the serial communication functions.

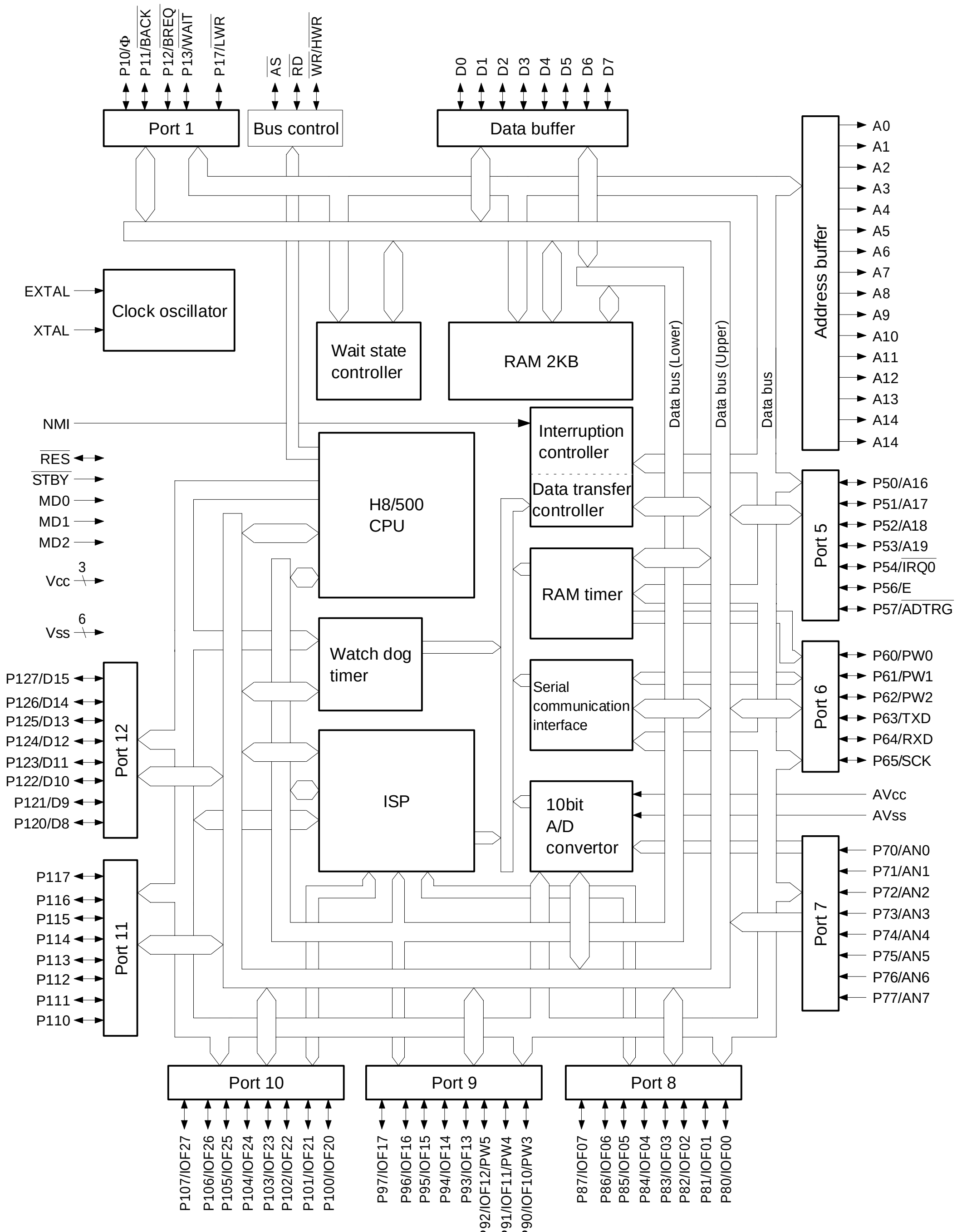
Major functions

- ISP (Built in the EPROM)
- SCI (Serial communication interface)
- PWM timer (pulse wide modulation)
- A/D convertor
- Watch-dog timer
- I/O port
- Built-in memory RAM (2KB)

③ Pin arrangement



④ **Internal block diagram**



⑤ **CPU pin signals**

Pin No.	Port	Signal name	In/Out	H/L	Specification
1	P90	TXD SUB	OUT	L	Serial data output to SUB CPU
2	P91	RXD SUB	IN	L	Serial data input from SUB CPU
3	P92	TXD ICU	OUT	L	Serial data input to ICU
4	P93	RXD ICU	IN	L	Serial data output from ICU
5	P94	RES SUB	OUT	L	Reset signal to SUB CPU
6	P95	RES OPE	OUT	L	Reset signal to the operation panel
7	P96	RES ICU	OUT	L	Reset signal to ICU
8	P97	RES PRT	OUT	L	Reset signal to the printer
9	VCC	VCC			Power 5V
10	P100	TXD OPE	OUT	L	Serial data output to the operation panel
11	P101	RXD OPE	IN	L	Serial data input from the operation panel
12	P102	TXD PRT	OUT	L	Serial data output to the printer
13	P103	RXD PRT	IN	L	Serial data input from the printer
14	P104	—	—	—	Not used.
15	P105	—	—	—	Not used.
16	P106	TXD RIC	OUT	L	Serial data output to RIC
17	P107	RXD RIC	IN	L	Serial data input from RIC
18	P80	—	—	—	Not used.
19	P81	—	—	—	Not used.
20	P82	—	—	—	Not used.
21	P83	—	—	—	Not used.
22	P84	—	—	—	Not used.
23	P85	PRTCHin	IN	L	Printer PWB detection signal
24	P86	—	—	—	Not used.
25	P87	—	—	—	Not used.
26	VSS	VSS			Power GND
27	P120	DSR SUB	IN	H	Request signal from SUB
28	P121	DSR ICU	IN	H	Request signal from ICU
29	P122	DSR OPE	IN	H	Operation panel request signal
30	P123	DSR PRT	IN	H	Printer request signal
31	P124	—	—	—	Not used.
32	P125	DSR RIC	IN	L	DSR from RIC (Power confirmation signal)
33	P126	CTS RIC	IN	L	CTS for RIC (Send request signal)
34	P127	READY	IN	H	Polygon motor ready signal
35	VSS	VSS			Power GND
36	D0	D0			Data signal
37	D1	D1			Data signal
38	D2	D2			Data signal
39	D3	D3			Data signal
40	D4	D4			Data signal
41	D5	D5			Data signal
42	D6	D6			Data signal
43	D7	D7			Data signal
44	VCC	VCC			Data signal
45	A0	A0			Address signal
46	A1	A1			Address signal
47	A2	A2			Address signal
48	A3	A3			Address signal
49	A4	A4			Address signal
50	A5	A5			Address signal
51	A6	A6			Address signal
52	A7	A7			Address signal
53	VSS	VSS			Power GND
54	A8	A8			Address signal
55	A9	A9			Address signal
56	A10	A10			Address signal

Pin No.	Port	Signal name	In/Out	H/L	Specification
57	A11	A11			Address signal
58	A12	A12			Address signal
59	A13	A13			Address signal
60	A14	A14			Address signal
61	A15	A15			Address signal
62	A16	A16			Address signal
63	A17	A17			Address signal
64	A18	A18			Address signal
65	A19	A19			Address signal
66	P13	—	—	—	Not used.
67	P12	—	—	—	Not used.
68	P11	—	—	—	Not used.
69	P10	—	—	—	Not used.
70	RES	RES	IN	L	Reset signal
71	NMI	—	—	—	Not used.
72	VSS	VSS			Power GND
73	EXTAL	EXTAL	IN		Clock 19.6608MHz
74	XTAL	XTAL	IN		Clock 19.6608MHz
75	VCC	VCC			Power 5V
76	$\overline{AS}$	ASM	OUT		Address strobe signal
77	$\overline{RD}$	ROM	OUT		ROM, RAM I/O data read signal
78	$\overline{WR}$	WRM	OUT		ROM, RAM I/O data write signal
79	P17	—	—	—	Not used.
80	MD0	MD0	IN	L	Operation mode control signal
81	MD1		IN	H	Operation mode control signal
82	MD2		IN	H	Operation mode control signal
83	$\overline{STBY}$		IN	H	Hardware standby mode signal
84	AVCC	AVCC	IN		A/D convertor reference power pin
85	P70	—	—	—	Not used.
86	P71	AN1 (GND)			GND2
87	P72	AN2 (GND)			GND2
88	P73	AN3 (GND)			GND2
89	P74	AN4 (GND)			GND2
90	P75	AN5 (GND)			GND2
91	P76	AN6 (GND)			GND2
92	P77	AN7 (GND)			GND2
93	AVSS	AVSS			GND2
94	VSS	VSS			GND2
95	P57	—	—	—	Not used.
96	P56	—	—	—	Not used.
97	P54	POFA	IN		Power OFF signal
98	P60	DCH	OUT	H	
99	P61	MSWR	OUT	H	Main switch relay signal
100	P62	DFM	OUT	H	Power fan motor signal
101	P63	OPTS	OUT	L	IR output signal
102	P64	OPTR	IN	L	IR input signal
103	P65	—	—	—	Not used.
104	VSS	VSS			POWER GND
105	P110	DTR SUB			DTR for SUB
106	P111	DTR ICU			DTR for ICU
107	P112	DTR OPE			DTR for the panel
108	P113	DTR PRT			DTR for the printer
109	P114	—	—	—	Not used.
110	P115	DTR RIC	OUT	H	DTR for RIC (Power confirmation signal)
111	P116	RTS RIC	OUT	H	RTS for RIC (send enable)
112	P117	START			Polygon motor rotation pin

(2) RAM (AT28C64)

① Outline

The RAM stores various setting data required for operations of the AR-5132 system, causes of paper jams, and the counter data such as trouble codes. (Batteries are not required.) Data transmission is performed between the RAM and the main PWB immediately after turning ON or OFF the power.

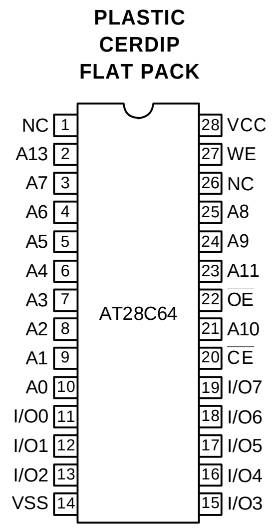
The AT28C64 is an EEPROM (Electrically Erasable ROM) of 8KByte and operates on a single power source of 5V.

② Features

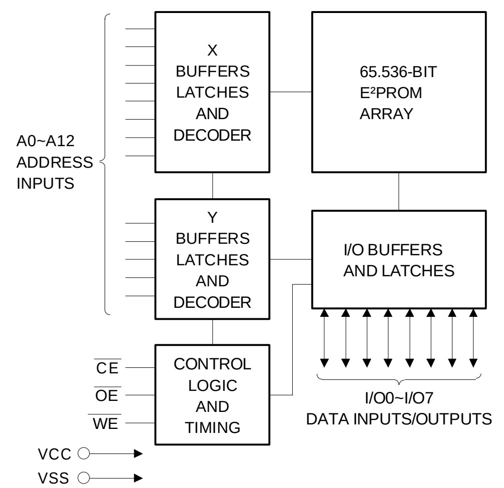
Low power CMOS operating current max. 60mA

All memory write time: Average 0.625sec

③ Pin arrangement



④ Internal block diagram



⑤ RAM (IC115) pin signals

Pin No.	In/Out	Signal name	Function
1	—	NC	
2	IN	A12	Address signal
3 ~ 10	IN	A7 ~ A0	Address signal
11 ~ 13	IN/OUT	1/00 ~ 1/02	Data signal
14	—	GND	GND (0V)
15 ~ 19	IN/OUT	1/03 ~ 1/07	Data signal
20	IN	$\overline{CS}$	RAM chip select signal. RAM is selected at LOW (0V).
21	IN	A10	Address signal
22	IN	$\overline{RD}$	Read signal. RAM data are read into the CPU at LOW.
23	IN	A11	Address signal
24	IN	A9	Address signal
25	IN	A8	Address signal
26	IN	NC	
27	IN	$\overline{WR}$	Write signal. Date are written into the RAM from the CPU at LOW (0V).
28	—	5V	Power source. @ medium index = (3) start/stop control circuit

(3) Start/stop control circuit

① Outline

The ON/OFF state of the power is detected to control start/stop of each circuit.

The DC power PWB supplies the power voltages (VB = +24V, VC = +10V, VD1 = 5V, VD2 = 5V).

When the power voltage reaches the specified level, the operation of each circuit is started. Before the power voltage falls below the specified level, the operation is stopped, preventing malfunctions.

② Operation

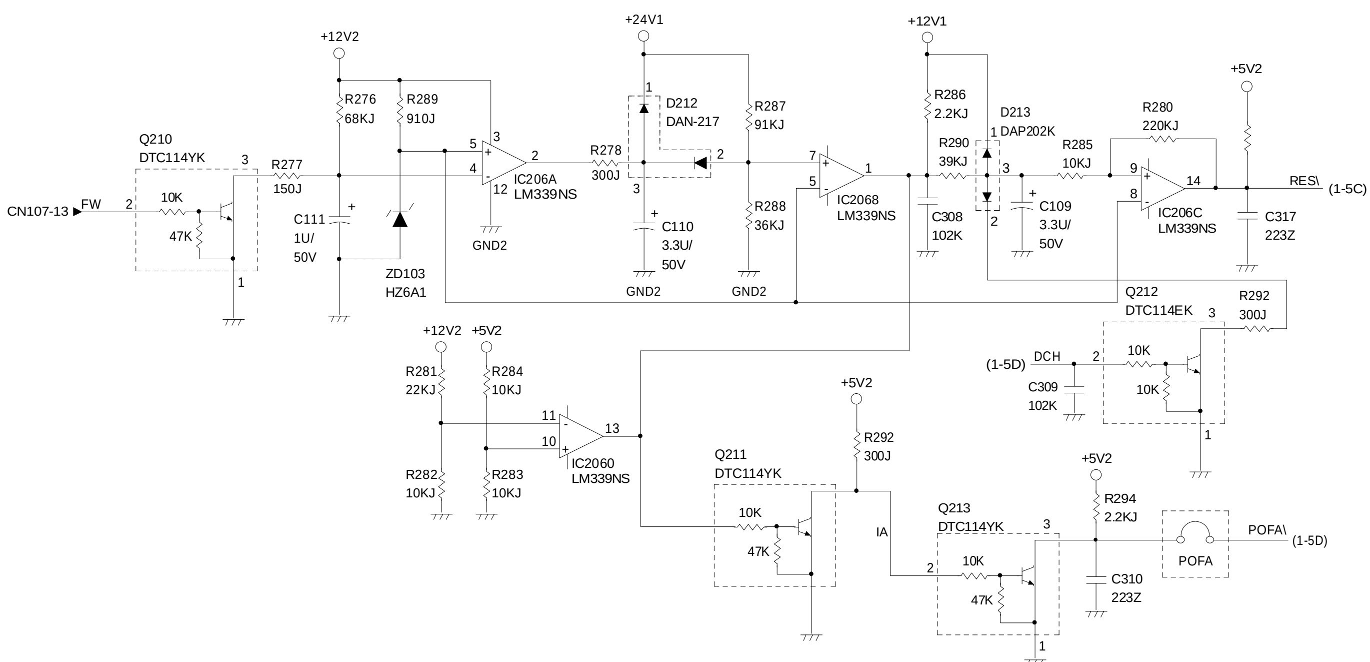
a. POFA generation circuit (Power voltage detection circuit)

This circuit detects ON/OFF of the power and the power voltage. The Immediately after turning on the power, when the AC input voltage is abnormally low, in case of an instantaneous service interruption, in the transient period after turning off the power, the DC power is low and unstable.

When the DC power voltage falls below the specified level, the circuits will not operate normally. Especially immediately after turning on/off the power, data transmission is performed between the EEPROM (IC118) and the CPU (IC107). @IN1/ = If the power voltage is +5V lower, data transmission is not performed.

To prevent against this state, ON/OFF of the power is detected in an early stage and informed to the CPU; data transmission between the CPU and the RAM and the operations of the circuits are started after the DC power voltage reaches the machine operatable level; data transmission between the CPU and the RAM is completed before the DC power voltage falls below the machine operation impossible level; and the operations of the circuits are stopped. (Data transmission between the CPU and the EEPROM is allowed unless the +5V3 voltage does not fall.)

The POFA signal informs the CPU of ON/OFF of the power and the DC power state in the circuit. The POFA is driven HIGH (+5V) when the power is turned on and the DC power rises above the specified level. When the power is turned off, it is driven LOW (0V) before the DV power voltage falls below the specified level.

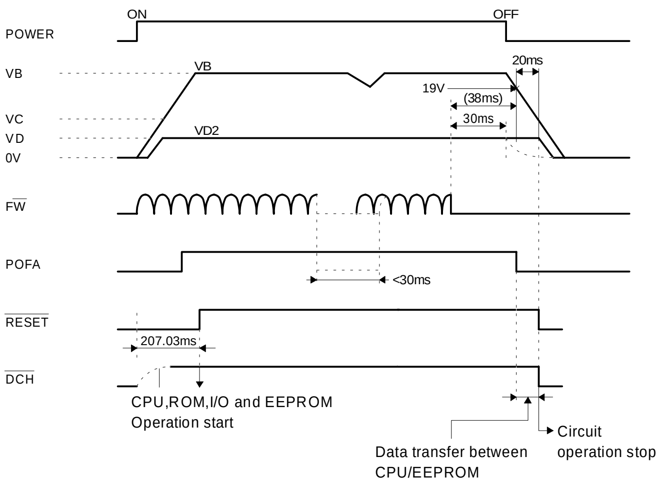


b. $\overline{\text{RESET}}$ generation circuit

The $\overline{\text{RESET}}$ signal is formed by the power voltage detection signal (POFA) and the data transfer complete signal ($\overline{\text{DCH}}$) from the CPU. It is used to operate the circuits in the DC power voltage stable area.

The $\overline{\text{RESET}}$ signal is set (the operation enable state) when the $\overline{\text{POFA}}$ becomes HIGH (+5V). It is reset (the operation stop state) when the $\overline{\text{DCH}}$ becomes LOW (0V).

Besides, when the $\overline{\text{POFA}}$ becomes LOW, data are transmitted from the $\overline{\text{CPU}}$ to the EEPROM. After completion of data transmission, the $\overline{\text{DCH}}$ becomes LOW.



c. Operation at power ON

- Immediately after power ON, the FW rises to turn on the collector and the emitter of Q210.
  Since the IC206 4pin voltage becomes about 0.736V, which is lower than the 5pin voltage (ZD103: 5.2 ~ 5.5V), and 2pin is open.
- The 24V rises after about 16msec from rising of the FW and C110 is charged through R287 and D212. In about 95msec, the IC206 7pin voltage becomes higher than the IC206 5pin (ZD103: 5.2 ~ 5.5V) and 1pin becomes HIGH.
- The IC206 1pin becomes HIGH to turn on the collector and the emitter of Q211. The Q211 collector becomes LOW to turn off Q213. The POFA is driven HIGH through R294.

d. Operations at power OFF

- Immediately after power OFF, the FW rises to open the collector and the emitter of Q210, and C111 is charged through R276. In about 30msec, the IC206 4pin voltage becomes higher than 5pin (ZD103: 5.2 ~ 5.5V) to drive 2pin LOW.
- The 24V starts rising about 16msec behind from FW. IC110 is charged through R287 and D212. The IC206 7pin voltage becomes higher than the reference voltage of the IC206 5pin (ZD103: 5.2 ~ 5.5V), and the 1pin voltage becomes HIGH.
- The IC206 1pin becomes LOW to turn off Q211. The High level is inputted to Q213 through R291 to turn on and to drive the POFA LOW.

e. Operations at instantaneous service interruption

Since the POFA signal is outputted from IC206, the POFA signal may be erroneously delivered due to the difference in rising time of 5V and 12V power. Therefore the power voltages of 5V and 12V are monitored by IC206 to control the POFA signal.

- When the power is turned OFF, the POFA signal must be driven LOW (0V) in an early stage. If, however, it is driven low too early, the machine will stop at an instantaneous service interruption (30msec or less) which does not affect the machine operations. Therefore in this circuit, if the AC power is turned off continuously for more than 30msec, it is judged as power OFF and the POFA is driven LOW.
- In normal operation, the IC206 4pin voltage is LOW. In an instantaneous service interruption, the FW becomes LOW immediately to open the collector and the emitter of Q210, charging C111 through R276. It takes 30msec for the IC206 4pin voltage to rise above the reference voltage (IC206 5pin 5.2 ~ 5.5V). In an instantaneous service interruption below 30msec, the machine will not stop.

f. Operations when the power voltage falls

- When the AC power voltage falls below the specified level, the DC power voltage falls though the DC power circuit is the regulator circuit.
  Then the 24V voltage is detected, and when it falls below 19V, the POFA is driven LOW (0V). (When it falls below 19V, the IC206 5pin voltage is divided by R287 and R288 to be lower than the reference voltage of 9pin. Therefore the comparator (IC206) output becomes LOW.)

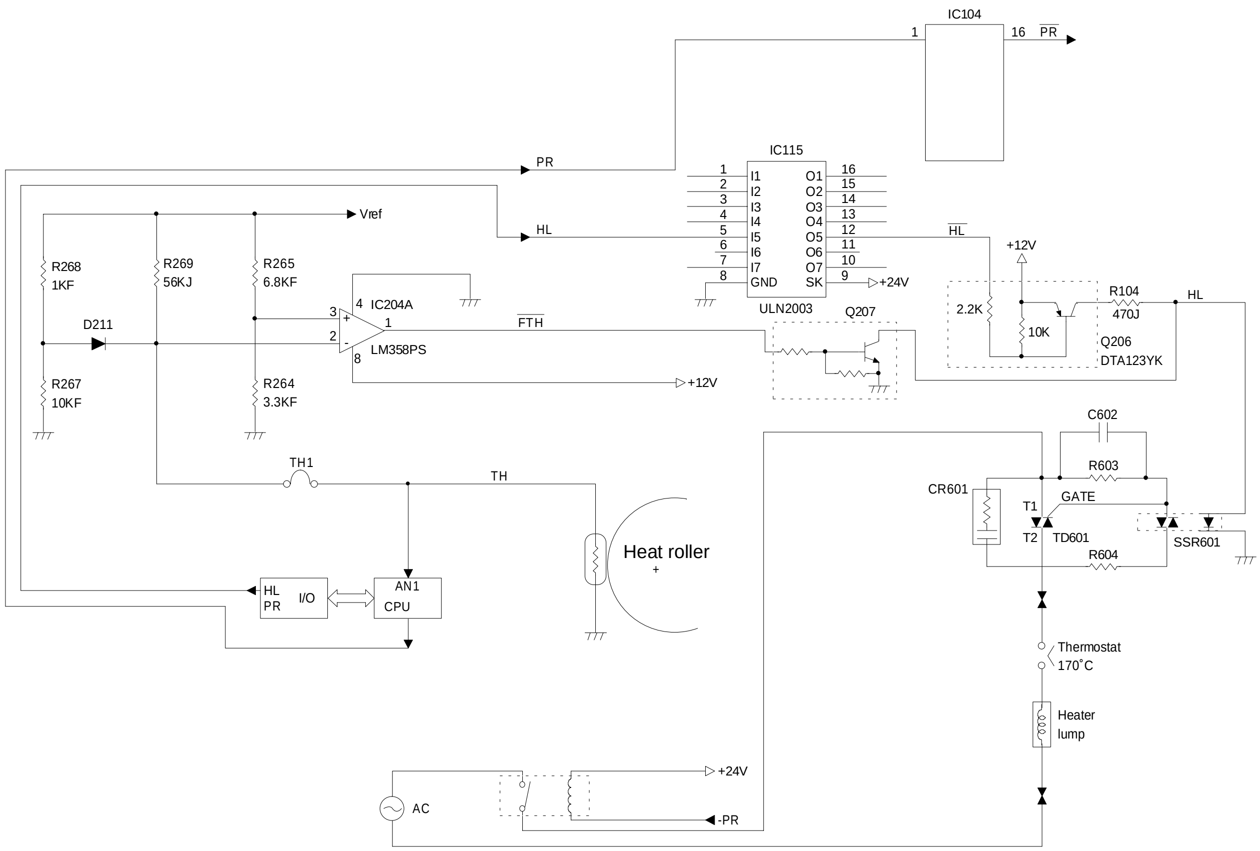
(4) Heater lamp control circuit

① Outline

The heater lamp control circuit detects the heat roller surface temperature by the thermistor and converts it into the voltage level (analog level) to output to the CPU analog input pin.

The CPU converts the analog voltage into a digital signal level and compares it with the set value of the test command and turns on/off the heater lamp to maintain the heat roller surface temperature at a constant level.

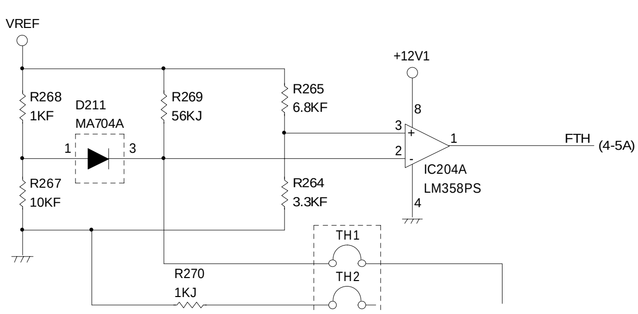
When a paper jam occurs in the AR-5132, the control circuit operates for max. 3 minutes to shorten the jam recovery time (8sec).



The thermistor resistance becomes greater when the heat roller surface temperature is lower, and becomes smaller when the surface temperature is higher. Therefore the thermistor pin voltage also becomes higher when the heat roller surface temperature is lower, and it becomes lower when the surface temperature is higher. The thermistor pin voltage in inputted to the CPU analog port. The CPU controls ON/OFF of the heater lamp by the input voltage level.

[High temperature protect circuit in case of hung up of the CPU]

The IC204 3pin (reference voltage) of +5V is divided by R265 and R264, and the thermistor pin voltage is inputted to the IC204 2pin. When, therefore, the 2pin voltage becomes lower than the 3pin voltage (the heat roller surface temperature about 230°C), the output 1pin becomes HIGH to turn on Q207, pulling the HL signal to the GND level and the heater lamp lighting signal is not generated.



[When the heat roller surface temperature is lower than the set level]

a. Since the thermistor pin voltage is higher than the set level, the output signal (HL) form the CPU becomes HIGH.

b. This HL signal becomes the $\overline{\text{HL}}$ signal through IC115 and TR Q206 and is inputted to the solid state relay (SSR).
When, therefore, the HL signal is HIGH, the internal triac is turned on.

c. When the internal triac is turned on, a pulse is applied to the gate of the external triac. A current flows from the power through the heater lamp to the triac to turn on the heater lamp.

[When the heat roller surface temperature becomes higher than the set level]

a. Since the thermistor pin voltage is lower than the set level, the output signal HL from the CPU becomes LOW.

b. The HL signal becomes LOW, SSR is OFF, the external triac is OFF, and the heater lamp is OFF.

[Q206]

This prevents the heater lamp from being always kept ON by the improper treatment of the harness for the heater lamp drive signal.

(5) Driver circuit (Solenoid, magnetic clutch)

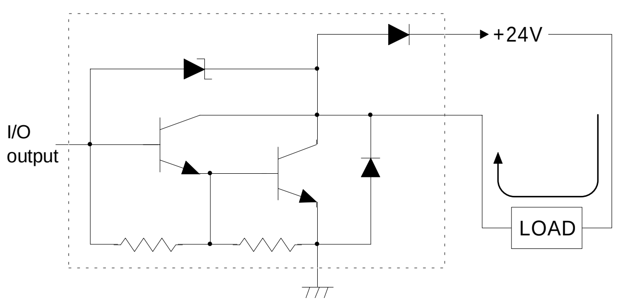
① Outline

The control signals of the loads outputted from the CPU I/O are unable to drive loads directly. They are passed through the driver IC to each load.

② Operation

The driver circuit composes the Darlington circuit with two transistors.

By this circuit, a great drive current is obtained from a small input current (I/O output current). When the driver input voltage is HIGH (+5V), the transistor turns on to flow a current in the arrow direction to operate the loads. When the driver is on, the driver output pin voltage is 0V.



(6) Stepping motor drive circuit

① Outline

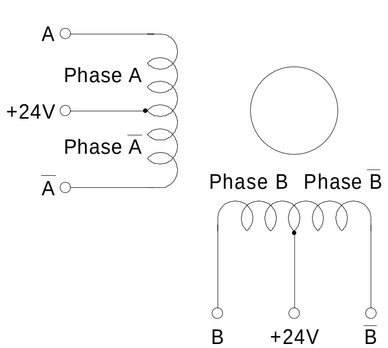
The driver circuit drives the auto duplex copy tray side plate motor and the rear edge motor.

A: Stepping motor A phase coil drive signal

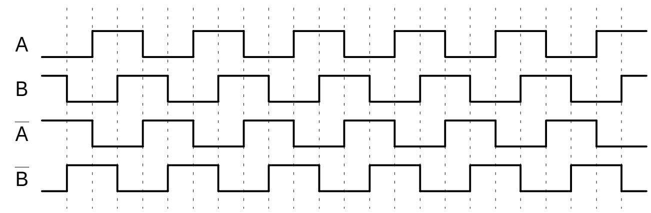
B: Stepping motor B phase coil drive signal

$\overline{A}$: Stepping motor A phase coil drive signal

$\overline{B}$: Stepping motor B phase coil drive signal



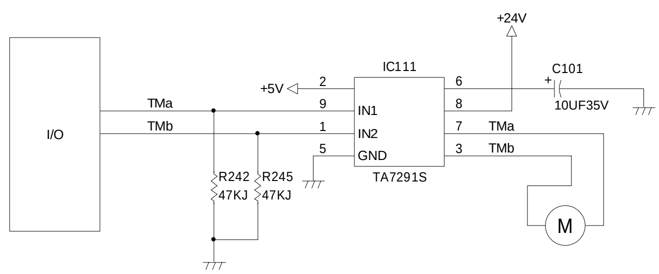
Stepping motor time chart



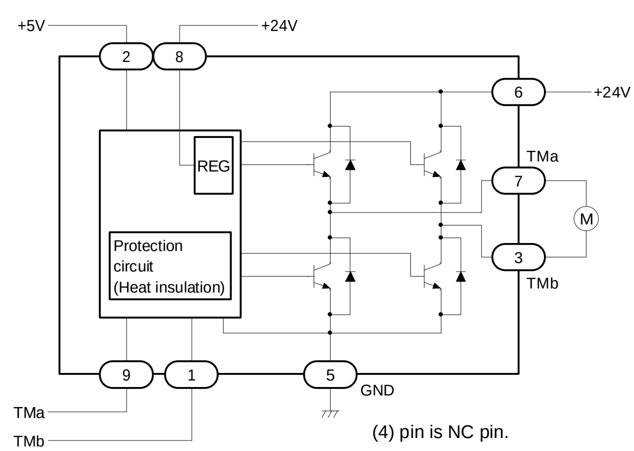
Drive signal	Side plate motor	Rear edge motor.
A	PAM1-0	PAM2-0
B	PAM1-1	PAM2-1
$\overline{A}$	PAM1-2	PAM2-2
$\overline{B}$	PAM1-3	PAM2-3

(7) Toner supply motor drive circuit

The IC111 is used to control the motor and to drive the toner supply motor with the pulse signals (TMa, TMb) outputted from the I/O chip.



Internal circuit



(4) pin is NC pin.

Truth value table

Input		Output		Mode
TMa	TMb	TMa	TMb	
L	L	∞	∞	Stop
H	L	H	L	CW/CCW
L	H	L	H	CCW/CW
H	H	L	L	Brake

∞ : High impedance

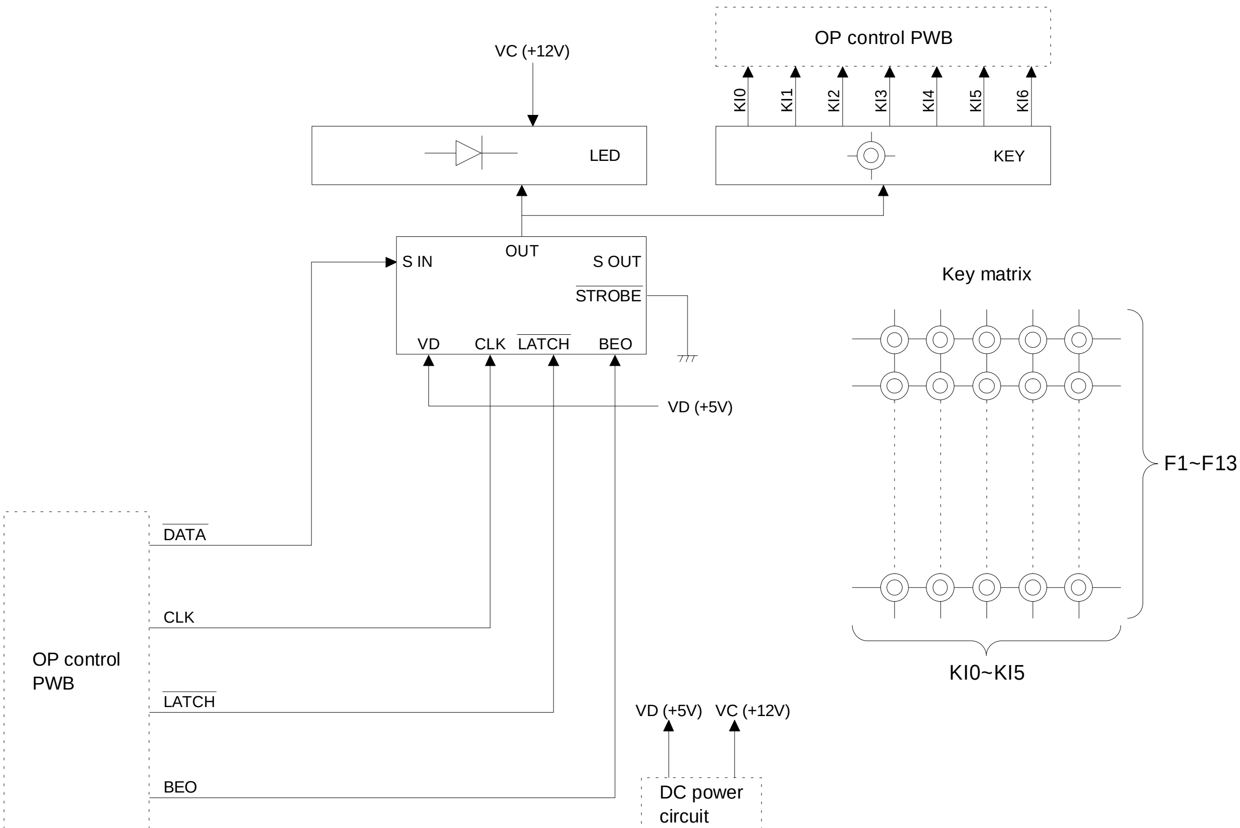
4. Operation section

(1) Outline

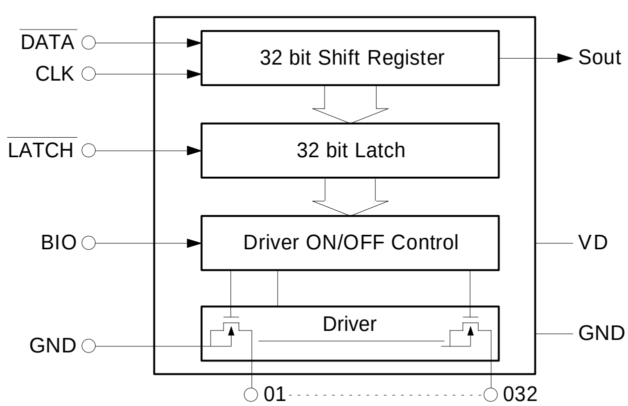
The operation circuit is composed of the key matrix circuit and the display circuit.

Besides, communication with is made with the IR unit.

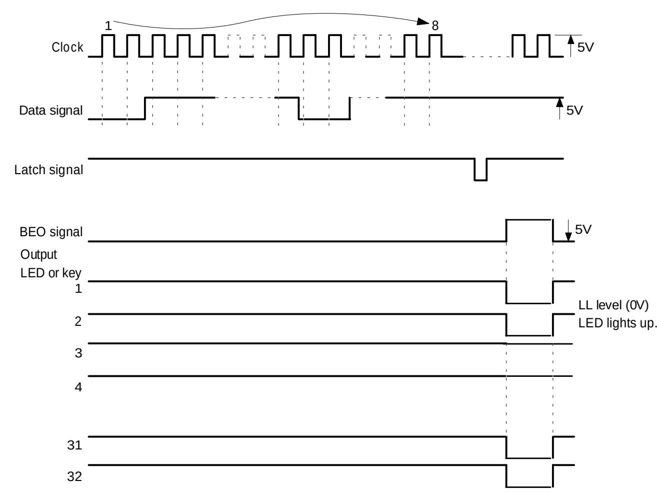
① Block diagram



32bit driver block diagram



② Operations

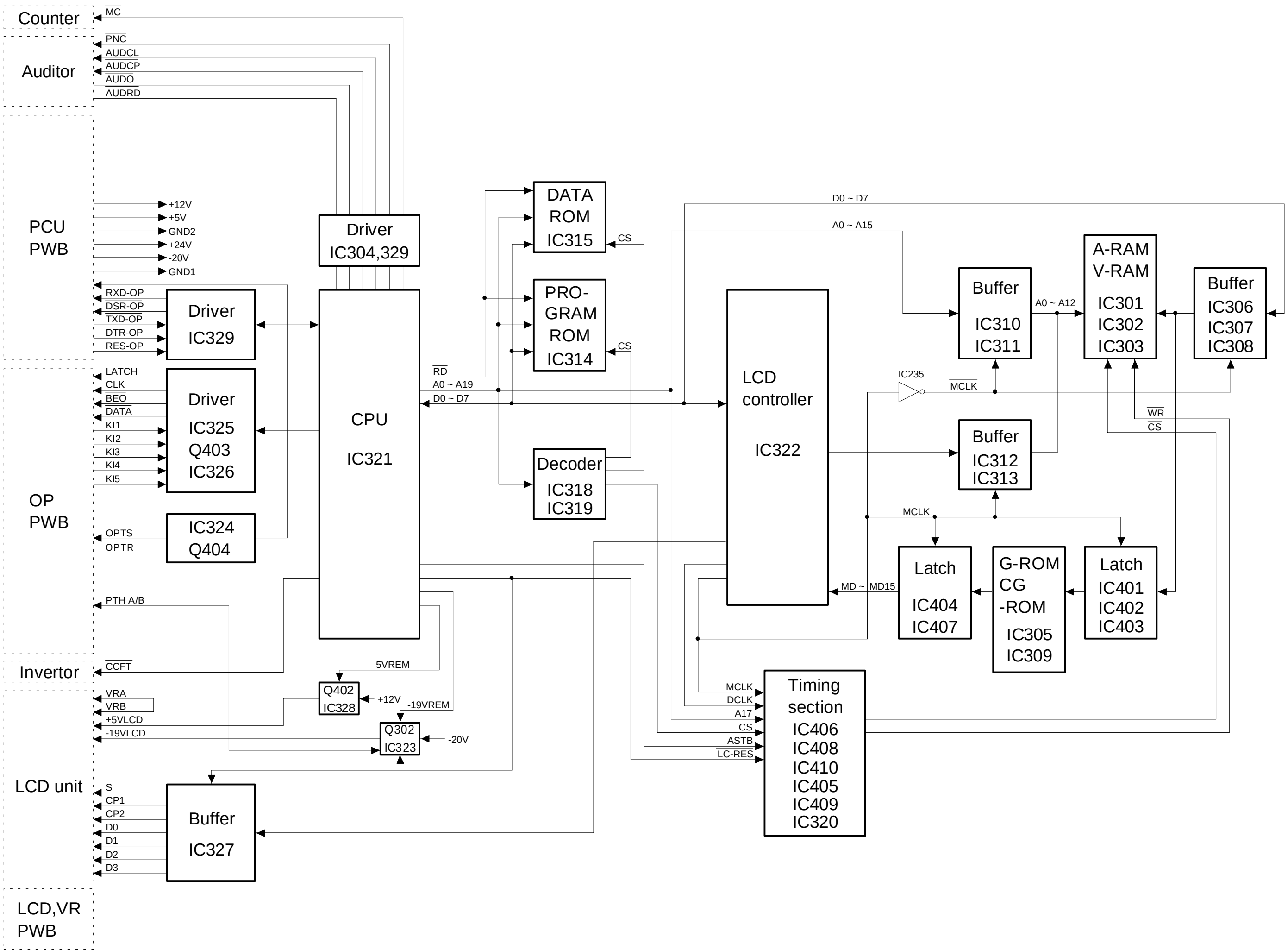


The data signal (8 bit) sent from the OP control PWB are shifted at the timing of rising of the clock and retained at the timing of rising of the latch signal.

The retained data are outputted when the BE0 signal becomes HIGH (5V) to light the LED or to select the key matrix (F1 ~ F13). Key reading is made by scanning K10 ~ K15 for every F1 ~ F13 selected.

5. LCD display section

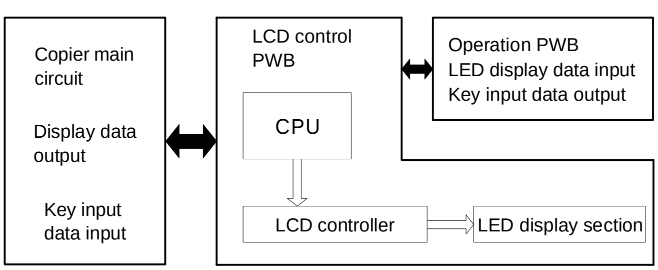
(1) Block diagram



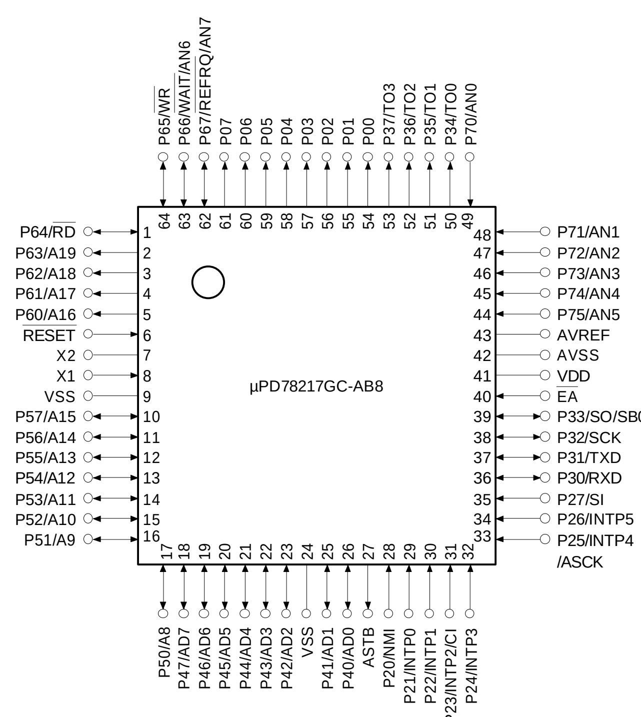
(2) CPU (IC321) µPD78217GC-AB8

① Outline

The CPU sends and receives data to and from the main circuit and the operation PWB through the serial data communication line, and controls the display system.



② Pin arrangement



③ CPU (IC322) pin signals

Pin No.	Signal name	In/Out	Function
1	$\overline{RD}$	OUT	Data read signal
2	A19		Address signal
3	A18		Address signal
4	A17		Address signal
5	A16		Address signal
6	$\overline{RESET}$	IN	Reset signal input from the main body main PWB
7	X2	—	CPU clock
8	X1	—	CPU clock
9	VSS		GND
10	A15		Address signal
11	A14		Address signal
12	A13		Address signal
13	A12		Address signal
14	A11		Address signal
15	A10		Address signal
16	A9		Address signal
17	A8		Address signal
18	AD7		Address data signal
19	AD6		Address data signal
20	AD5		Address data signal
21	AD4		Address data signal
22	AD3		Address data signal
23	AD2		Address data signal
24	VSS		GND
25	AD1		Address data signal
26	AD0		Address data signal
27	ASTB	OUT	Address latch signal
28	P20	—	Not used.
29	KI1	IN	Key input data
30	KI2	IN	Key input data
31	KI3	IN	Key input data
32	KI4	IN	Key input data

Pin No.	Signal name	In/Out	Function
33	KI5	IN	Key input data
34	K16	IN	Key input data
35	K10	IN	Key input data
36	TXD-OP	IN	Main communication (serial data output)
37	RXD-OP	OUT	Main communication (serial data input)
38	$\overline{CLK}$	OUT	LED clock
39	DATA	OUT	LED data
40	EA	—	Not used.
41	VDD		5V
42	AUSS		For analog port (GND)
43	AVREF		For analog port (5V)
44	P75	—	Not used.
45	DTR-OP	IN	Main communication DTR (send enable)
46	P73	—	Not used.
47	AUD	IN	Auditor counter presence/absence detection signal
48	PSEL	IN	Printer key page select signal
49	READY	IN	Auditor copy enable signal
50	P34	—	Not used.
51	LATCH	OUT	LED latch
52	BZR	OUT	Buzzer signal
53	$\overline{BEO}$	OUT	LED ON/OFF signal
54	PNC	OUT	Auditor, count-up signal
55	COPY	OUT	Auditor, copy state signal
56	CA	OUT	Auditor, clear all signal
57	DSR-OP	OUT	Main communication (Send request)
58	CCFT	OUT	Invertor ON/$\overline{OFF}$
59	– 19VREM	OUT	LCD-19V ON/$\overline{OFF}$
60	5VREM	OUT	LCD 5V ON/$\overline{OFF}$
61	LC-RES	OUT	LCD reset signal
62	P67	—	LCD reset signal
63	$\overline{WAIT}$	OUT	WAIT signal
64	$\overline{WR}$	OUT	Write signal (writing)

(3) ROM

① Outline

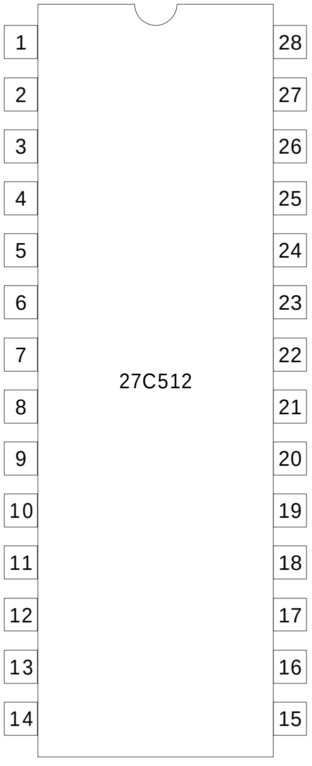
A. Program ROM (IC314)

B. Data ROM (IC315)

C. GROM (IC309) for storing graphic data

D. CGROM (IC305) for storing character data

② Pin arrangement (IC314)



③ ROM output signals (IC314)

Pin NO.	IN/OUT	Signal name	Function
1	IN	A15	Address signal
2	IN	A12	Address signal
3 ~ 10	IN	A7 ~ A0	Address signal
11 ~ 13	OUT	D0 ~ D2	Data signal
14	—	GND	GND (0V)
15 ~ 19	OUT	D3 ~ D7	Data signal
20	IN	CE	ROM chip enable signal. At LOW (0V), ROM data output enable.
21	IN	A10	Address signal
22	IN	$\overline{OD}$	Data output enable signal. At LOW, ROM data are sent to the CPU.
23	IN	A11	Address signal
24	IN	A9	Address signal
25	IN	A8	Address signal
26	IN	A13	Address signal
27	IN	A14	Address signal
28	—	5V	Power source

(4) Outline of LCD display control operations

① The CPU receives image data from the main body. (Besides, the key LED data are received.)

② With the received image data (corresponding to the data ROM address), the character data of the data ROM (corresponding to CG-ROM address) and graphic data (corresponding to G-ROM address) are read.

CG-ROM...... Character storing ROM

G-ROM .... Graphic storing ROM

③ The upper address and the lower address of the CG-ROM and the G-ROM corresponding to characters and graphic are written into the image areas of two V-RAM's.

Inversion and blink data corresponding to characters are written into the A-RAM (attribute RAM).

④ The LCTC (LCD controller) the LCTC (LCD controller), by using the G-ROM and the CG-ROM, allows to stock image dato of several screens in the V-RAM.

⑤ The read image data are transferred to the LCD unit.

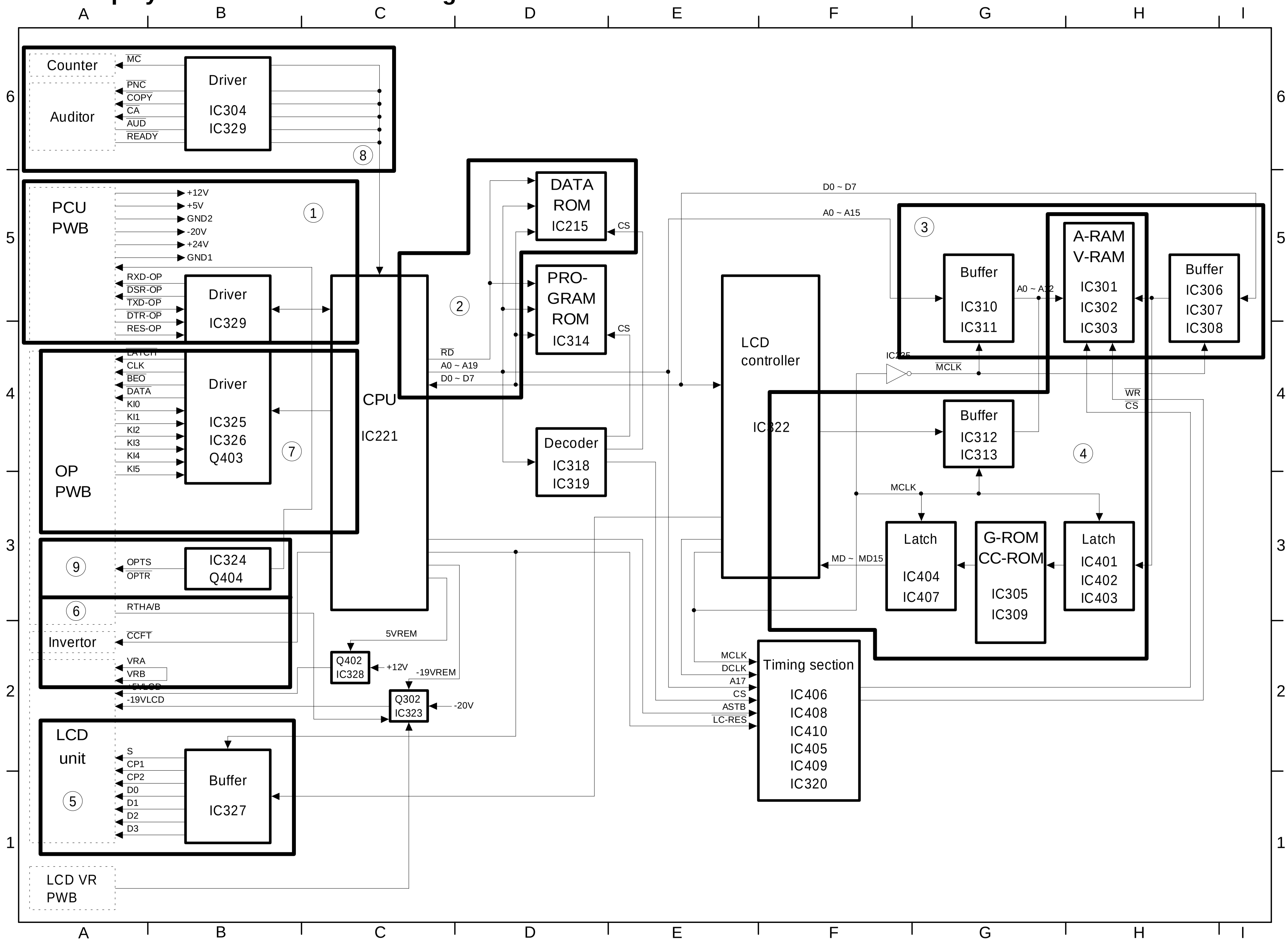
⑥ The LCD contrast is controlled by the thermistor.

⑦ Communication with the operation PWB

⑧ Interfaces the communication between Zaurus and the PCU PWB.

LCD display control section block diagram

LCD display control section block diagram



(5) LCD controller (IC322)

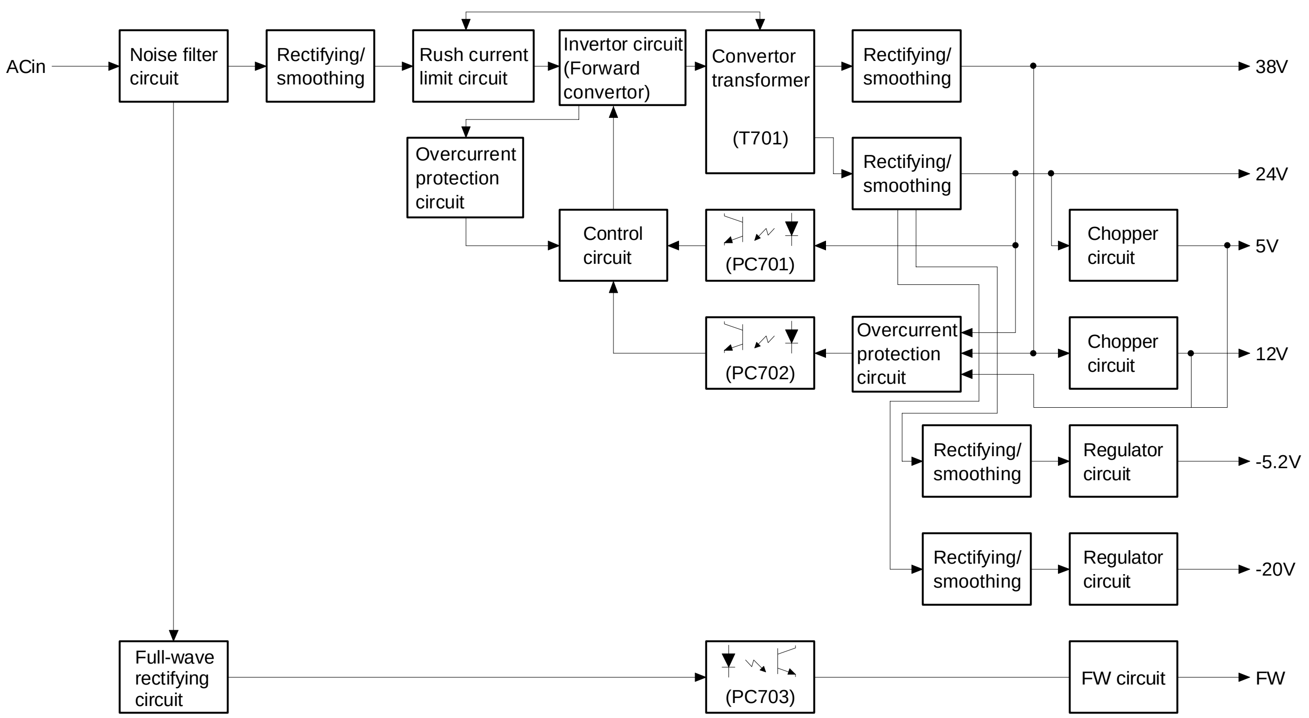
Pin No.	Signal name	In/Out	H/L	Function
1	MD0	IN		Character generation character out data
2	MD1	IN		Character generation character out data
3	MD2	IN		Character generation character out data
4	MD3	IN		Character generation character out data
5	MD4	IN		Character generation character out data
6	MD5	IN		Character generation character out data
7	MD6	IN		Character generation character out data
8	MD7	IN		Character generation character out data
9	MD8	IN		ARAM attribute code data
10	MD9	IN		ARAM attribute code data
11	MD10	IN		ARAM attribute code data
12	MD11	IN		ARAM attribute code data
13	MD12	IN		ARAM attribute code data
14	MD13	IN		ARAM attribute code data
15	MD14	IN		ARAM attribute code data
16	MD15	IN		ARAM attribute code data
17	VCC1			Power (5V)
18	—			
19	—			
20	—			
21	—			
22	LU3	OUT		Image data on LCD
23	LU2	OUT		Image data on LCD
24	LU1	OUT		Image data on LCD
25	LU0	OUT		Image data on LCD
26	M	OUT	H	LCD drive output AC conversion signal
27	FLM	OUT	H	Timing signal showing start of one frame
28	CL1	OUT	H	Display data latch signal
29	CL2	OUT	H	Display data shift signal
30	SK0	IN	H	Signal to use the IC low speed ROM/RAM when displaying a large screen.
31	SK1	IN	H	Signal to use the IC low speed ROM/RAM when displaying a large screen.
32	VCC2			Power source (5V)
33	DCLK	IN		Reference clock of internal operation of the LCD controller
34	MCLK	OUT		Clock showing the memory cycle
35	—			
36	—			
37	GND2			
38	$\overline{\text{RES}}$	IN	L	Reset signal for the LCD controller
39	$\overline{\text{CS}}$	IN	L	Signal to make access to the internal register of the LCD controller.
40	RS	IN		Selection of the address register and the data register of the LCD controller.

Pin No.	Signal name	In/Out	H/L	Function
41	F ($\overline{\text{WR}}$)	IN	L	Stroke signal for the CPU to read/write from/to the internal register of the LCD controller.
42	R/W ($\overline{\text{RD}}$)	IN	L	Controls data transmission direction between the CPU and the LCD controller.
43	DB0			Data communication line between the LCD controller and the CPU
44	DB1			Data communication line between the LCD controller and the CPU
45	DB2			Data communication line between the LCD controller and the CPU
46	DB3			Data communication line between the LCD controller and the CPU
47	DB4			Data communication line between the LCD controller and the CPU
48	DB5			Data communication line between the LCD controller and the CPU
49	DB6			Data communication line between the LCD controller and the CPU
50	DB7			Data communication line between the LCD controller and the CPU
51	BLE	IN		Determines whether the character blank is effective or not in the character unit attribute.
52	MODE	IN		Used to specify the image mode.
53	ON/$\overline{\text{OFF}}$	IN		Used to turn on/off the LCD display.
54	WIDE	IN		Signal to select the normal display and the double width display.
55	D/$\overline{\text{S}}$	IN		Used to select screens.
56	LS	IN		Used to specify the large screen.
57	AT	IN		—
58	G/$\overline{\text{C}}$	IN		Signal to select the graphic display and the character display.
59	GND1			
60	RA4	OUT		Raster address output
61	RA3	OUT		Raster address output
62	RA2	OUT		Raster address output
63	RA1	OUT		Raster address output
64	RA0	OUT		Raster address output
65	MA15	OUT		Memory address output
66	MA14	OUT		Memory address output
67	MA13	OUT		Memory address output
68	MA12	OUT		Memory address output
69	MA11	OUT		Memory address output
70	MA10	OUT		Memory address output
71	MA9	OUT		Memory address output
72	MA8	OUT		Memory address output
73	MA7	OUT		Memory address output
74	MA6	OUT		Memory address output
75	MA5	OUT		Memory address output
76	MA4	OUT		Memory address output
77	MA3	OUT		Memory address output
78	MA2	OUT		Memory address output
79	MA1	OUT		Memory address output
80	MA0	OUT		Memory address output

6. DC power circuit

(1) Block diagram

This power circuit is composed of the main section and the copy lamp section. The AC power is rectified by the main section, and switching-transformed by the DC/DC convertor, and rectified and smoothed again to provide DC power voltages of the loads. The copy lamp section directly rectifies the AC power, which is then switching-transformed by the DC/DC convertor to provide the output voltage to change the lamp light quantity.



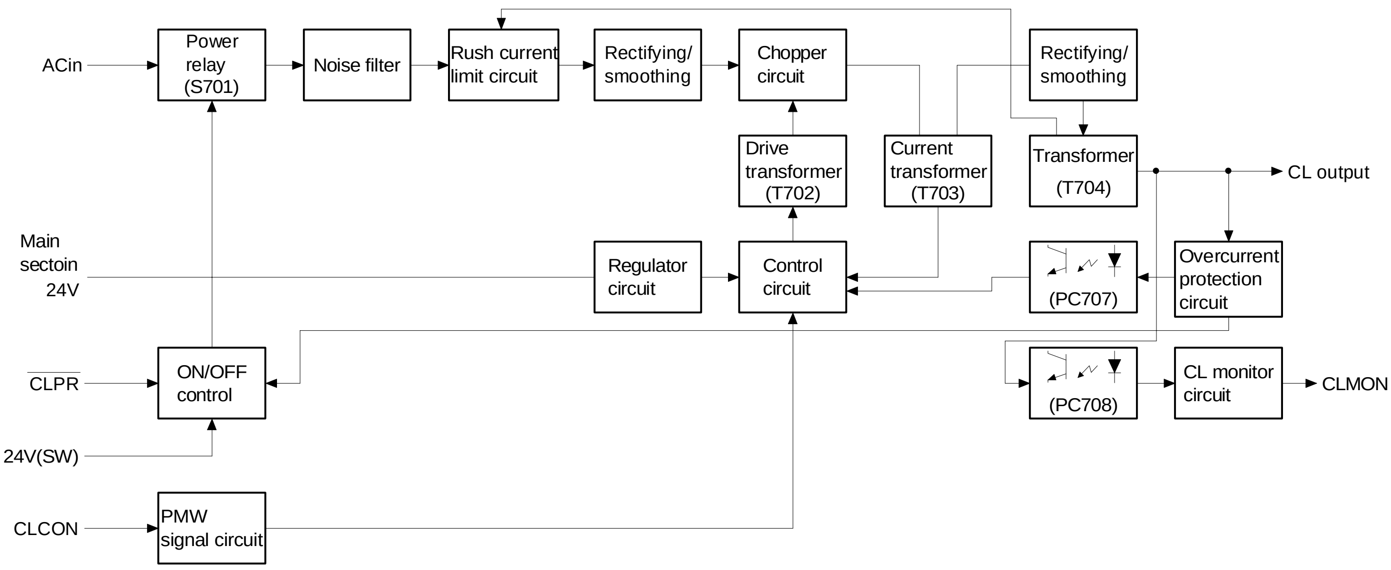


Fig. 1 Block diagram

(2) Circuit description

① Main circuit

a. Noise filter circuit

The noise filter circuit of the DC power is composed of L as shown in the figure below. It reduces the normal mode noises which come from the AC line.

The normal mode noises are noises which are overlapped in the AC line or the output line, and are attenuated by L701.

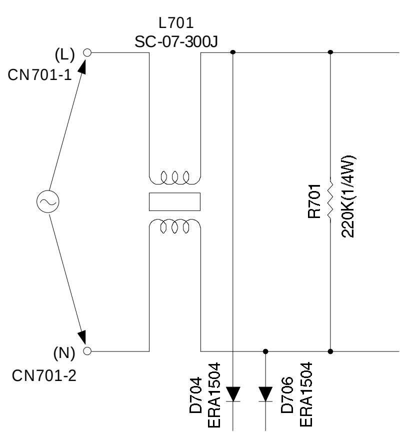


Fig. 2 Noise filter circuit

b. Rush current limit circuit

Since the AC power is directly rectified, without this circuit, en extremely great rush current would be generated by the charging current flowing to the smoothing capacitors (C707, C708) and the switch contact would be deteriorated.

To prevent against this, the circuit composed as follows is inserted between the rectifier diode (D701) and the smoothing capacitors (C707, C708) to limit the rush current. When the power is supplied, a charging current flows through R702 and FA701 to the smoothing capacitor so that the current at supplying the power is limited to 30A or less. (Fig. 3, Fig. 4)

After that, the smoothing capacitor voltage rises to operate the invertor circuit. Then the voltage generated in the convertor transformer triggers the triac (TR701) to ON. Therefore, in the normal operation, a current flows through TR701 and does not flow through T702 and FA701.

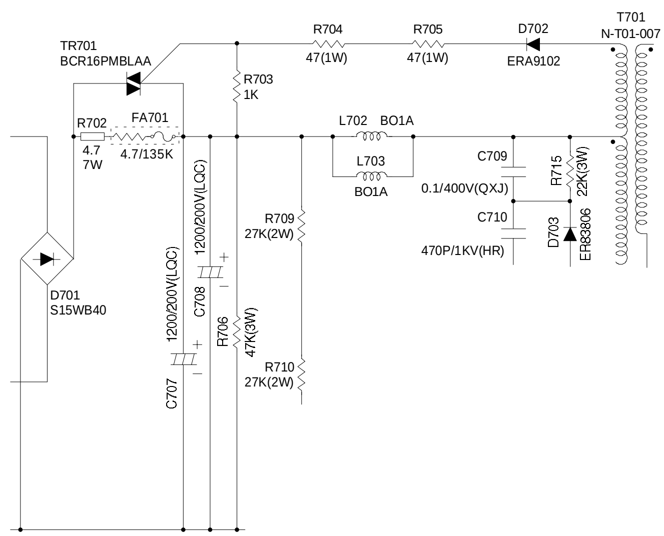


Fig. 3 Rush current limit circuit

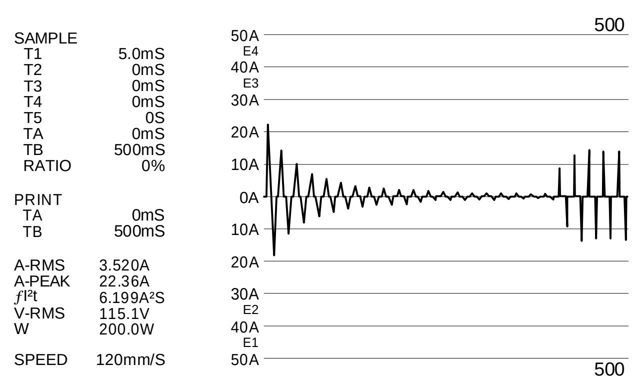


Fig. 4 Rush current

c. Rectifying/smoothing circuit

In this circuit, he AC voltage (50/60Hz) is rectified by the rectifier diode (D701) and smoothed by the smoothing capacitors (C707, C708). The solid line and the dotted line in the figure below show the flowing path of the charging current.

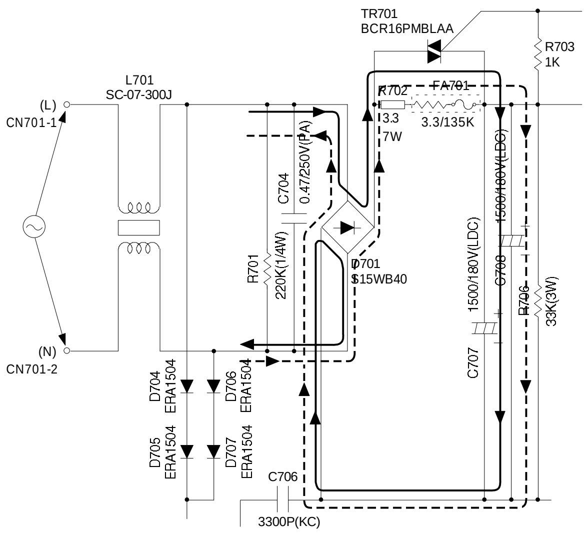


Fig. 5 Rectifying/smoothing circuit

d. Invertor circuit (Forward convertor)

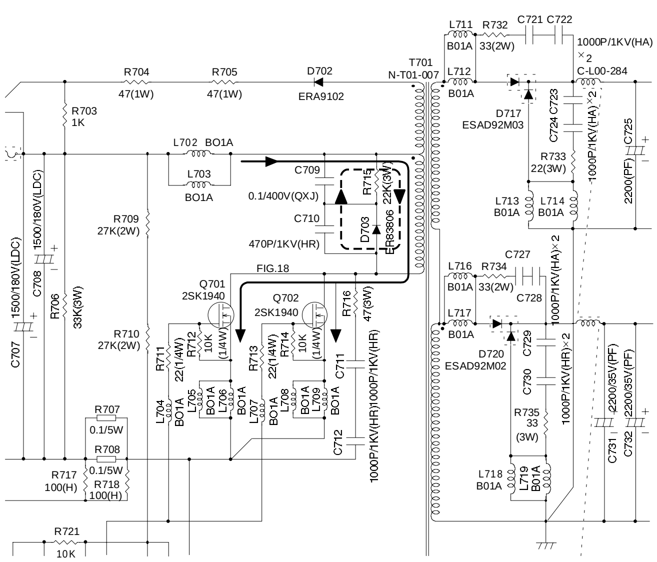


Fig. 6 Invertor circuit

In the forward convertor system, the FET (Q701, Q702) connected in series to the convertor transformer (T701) performs the ON/OFF switching operation. When in ON, energy is supplied to the secondary side through the convertor transformer. The DC current of the smoothing circuit is converted into the switching pulses by switching operation of the FET controlled by the single from the control circuit, and a high frequency power is supplied to the secondary side.

The solid line in the figure shows the current when the FET is turned on, and the dotted line shows the closed loop of the snubber circuit which absorbs a counter electromotive force generated in the convertor transformer.

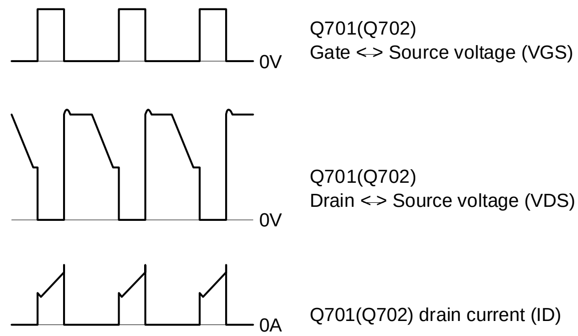


Fig. 7 Invertor operation waveform

e. Secondary side rectifying/smoothing circuit (24V, 38V series)

The voltage of the high frequency pulses generated by the invertor circuit is dropped by the convertor transformer (T701), rectified by the diode, and smoothed by the choke coil (L715) and the electrolytic capacitors (C725 in 38V series, C731 and C732 in 24V series).

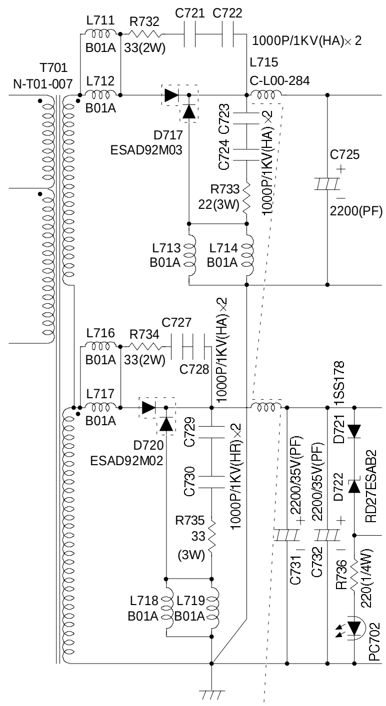


Fig. 8 rectifying/smoothing circuit

f. Control circuit

This circuit employs the power MOS FET as the switching element and the PWM control (Pulse Width Modulation) system by the primary side control. Therefore, the output in the secondary side (24V series) is detected by the output voltage detecting circuit, and the detected signal is fed back to the control IC (IC701) through the photo coupler (PC701) to change the pulse width of the switching FET in the primary side invertor circuit, stabilizing the output voltage.

g. Overcurrent protection circuit

The ⊖ line of the primary side is connected to the detecting resistor of the primary side current. When an overcurrent is generated, the current in the switching FET (Q701, Q702) is detected and a signal is sent to the control IC (IC701) to reduce the ON pulse width of the switching FET to reduce the output voltage. In this circuit, the switching FET is intermittently operated.

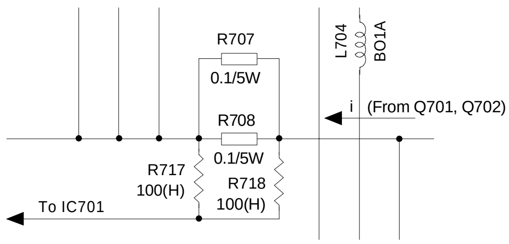


Fig. 9 Overcurrent protection circuit

h. Series regulator circuit (–5.2V series, –20V series)

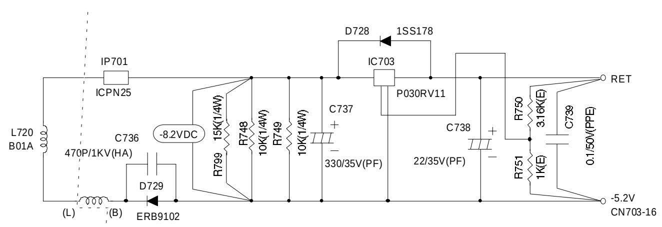


Fig. 10 Series regulator circuit (–5.2V)

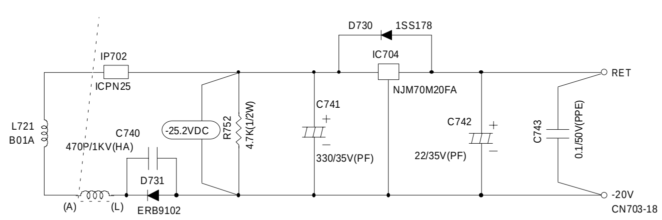
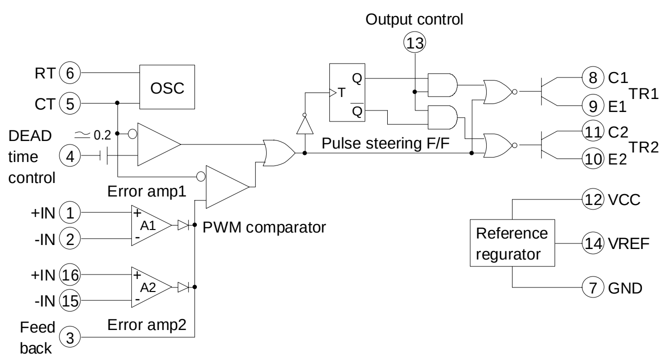


Fig. 11 Series regulator circuit (–20V)

This is also called the dropper system. The high frequency pulses from the choke coil (L715) are rectified and smoothed, and the voltage is dropped by the regulator IC to stabilize.

i. Chopper regulator circuit (5V series, 12V series)



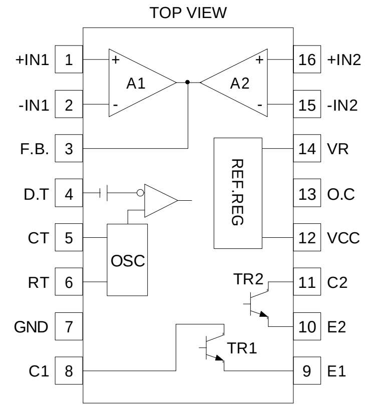


Fig. 12 IC705 (IC706) block diagram

The switching frequency is determined by the CR connected to the IC705 (IC706) 5pin and 6pin, and triangle waveforms of about 50KHz are generated.

The output voltage of the output voltage detecting circuit and the reference voltage (5V) at IC705 (IC706) 14pin are inputted to the error amplifier in each IC to control ON/OFF time of the output transistors TR1 and TR2 (PWM control), driving the switching FET Q706 (Q708) and stabilizing the output voltage.

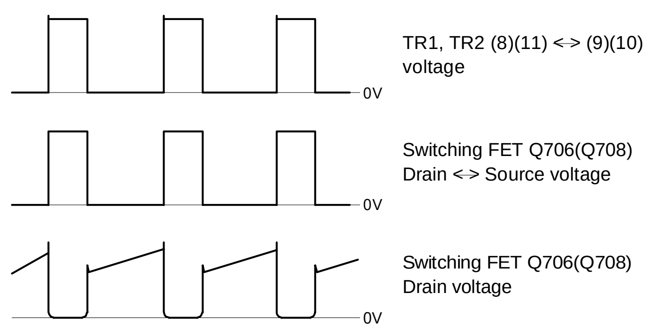


Fig. 13 Switching waveform of each section

j. FW signal

The AC input voltage is full-wave rectified by D704 ~ D707. Byturning ON/OFF Q703, the photo coupler is synchronized to performON/OFF operations.
This signal synchronized with the AC voltage waveform is transmitted to the secondary side by the photo coupler to turnON/OFF Q704 similarly, providing the FW signal synchronized withthe AC voltage waveform.

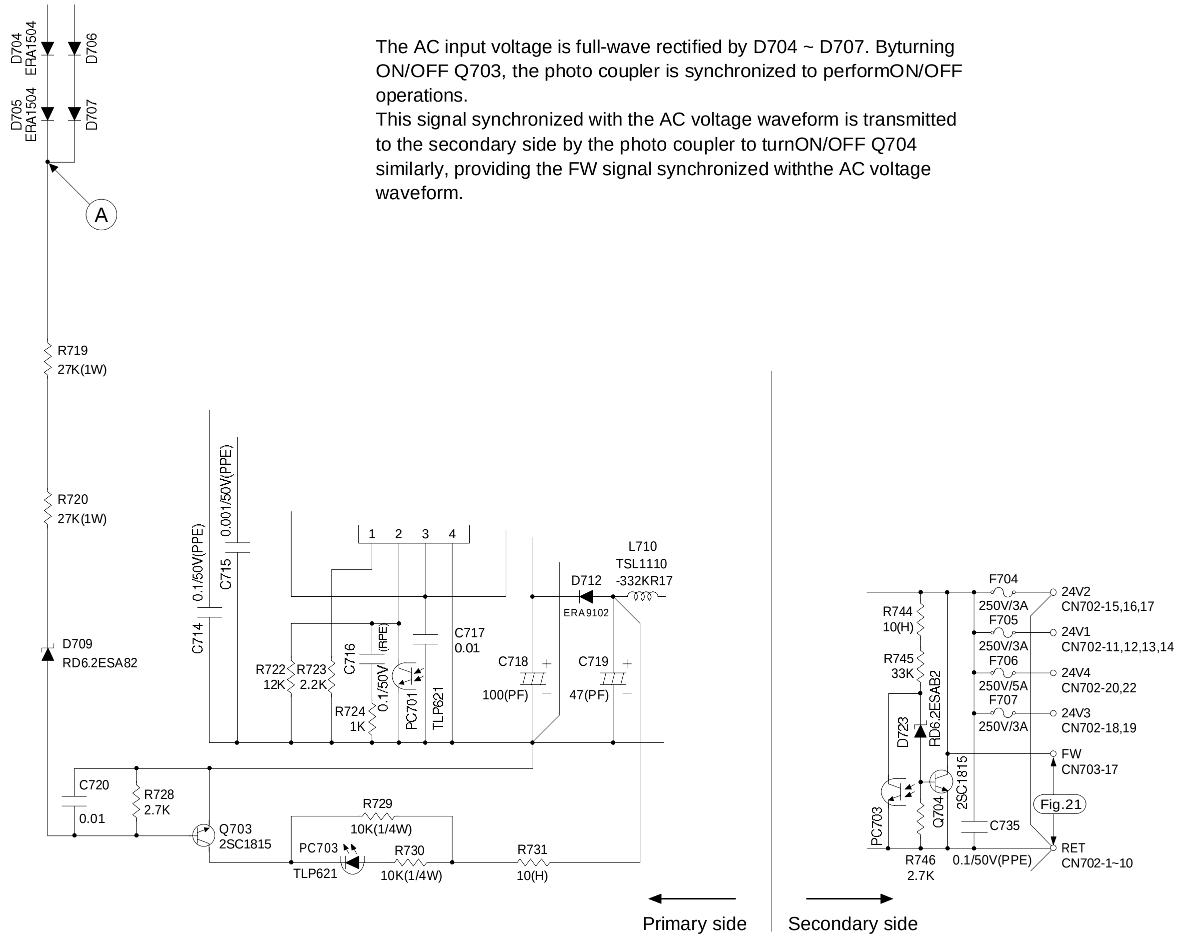


Fig. 14 FW signal circuit

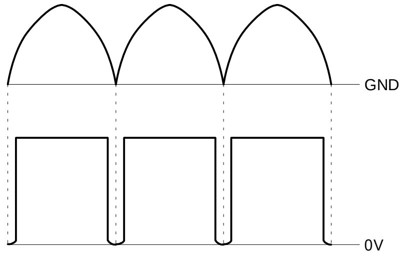


Fig. 15 Waveform of each section

k. Overvoltage protection circuit

When each output (excluding –5.2V and –20V series) becomes an overvoltage, the over voltage protection circuit of each output transmits a signal through the photo coupler (PC702) to the primary side control circuit, and the invertor operation is stopped by stopping the switching operation of IC701, preventing each output voltage from rising.

The operation is of latch system. After removing an overvoltage, apply the AC power to reset.

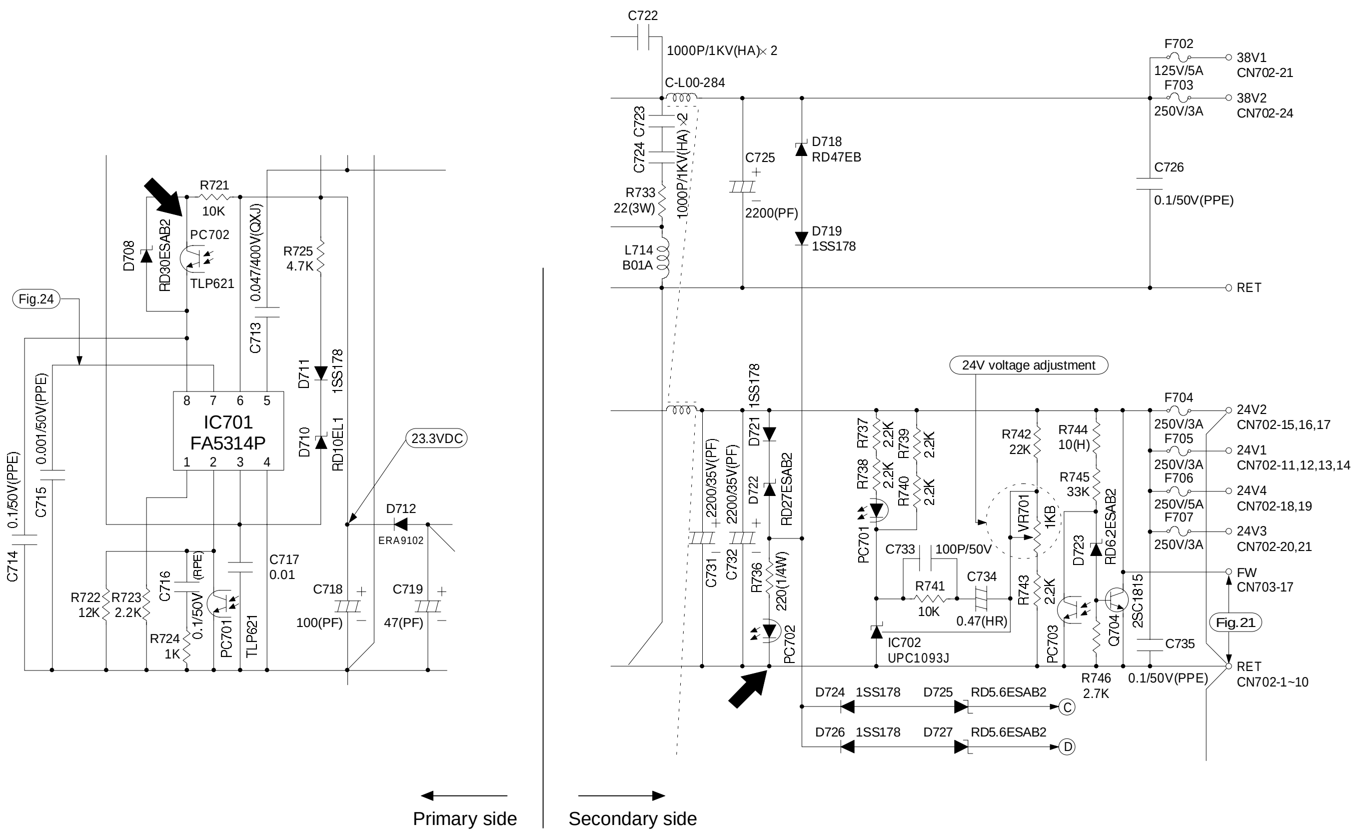


Fig. 16 Overvoltage protection circuit

l. Overheat protection circuit

The power unit is forcibly cooled by the cooling fan. In case of an abnormally high temperature due to the fan trouble, the temperature of the convertor transformer (T701) is detected by the temperature fuse (F710) to stop the switching operation of the power.

To reset, remove the abnormality and replace the fuse.

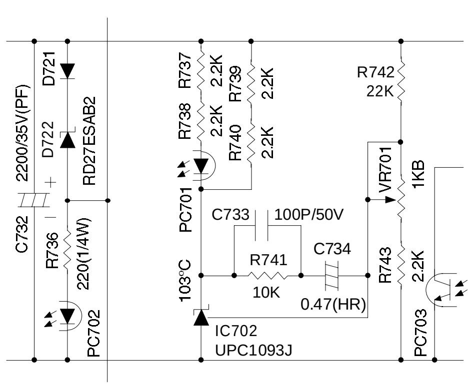


Fig. 17 Overheat protection circuit

[Waveform of each section]

Condition: Input 100V, 50Hz rated load

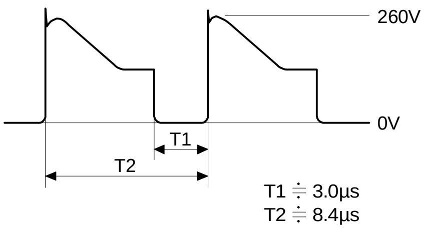


Fig. 18 Q701(Q702) drain-source voltage waveform

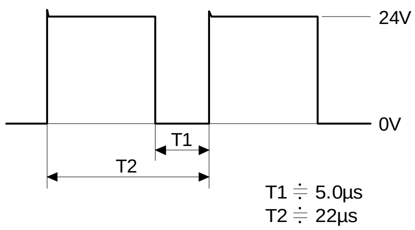


Fig. 19 Q706 drain-source voltage waveform

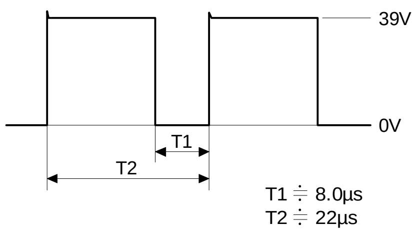


Fig. 20 Q708 Drain-source voltage waveform

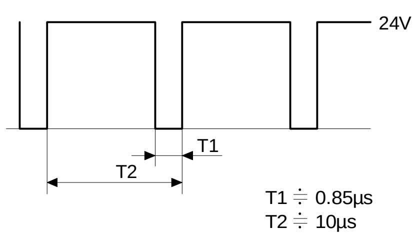


Fig. 21 FW signal waveform

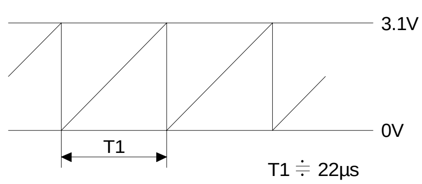


Fig. 22 IC7055 Pin OSC waveform

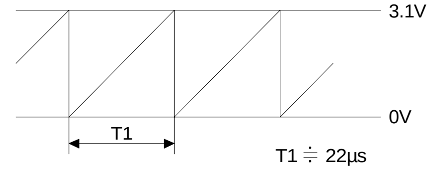


Fig. 23 IC7065 Pin PSC waveform

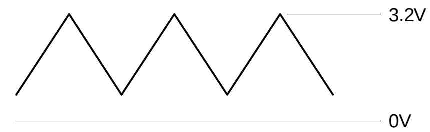


Fig. 24 IC701 Pin OSC waveform

② Copy lamp (CL) section

a. Noise filter circuit

Similarly to the main section, the noise filter circuit is composed of L and C as shown in the figure below. It reduces the normal mode noises and the common mode noises which come from the AC line.

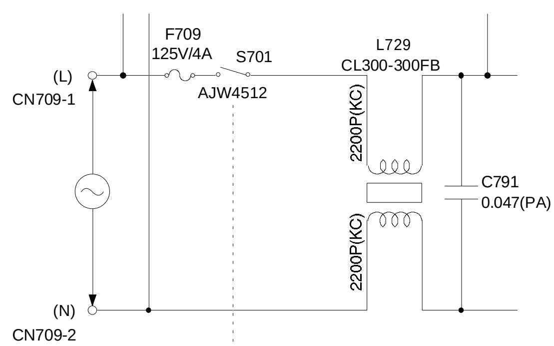


Fig. 32 Noise filter circuit

b. Rush current limit circuit

Similarly to the main section, the circuit shown below limits the rush current which flows into the smoothing capacitor (C792) when the power is supplied.

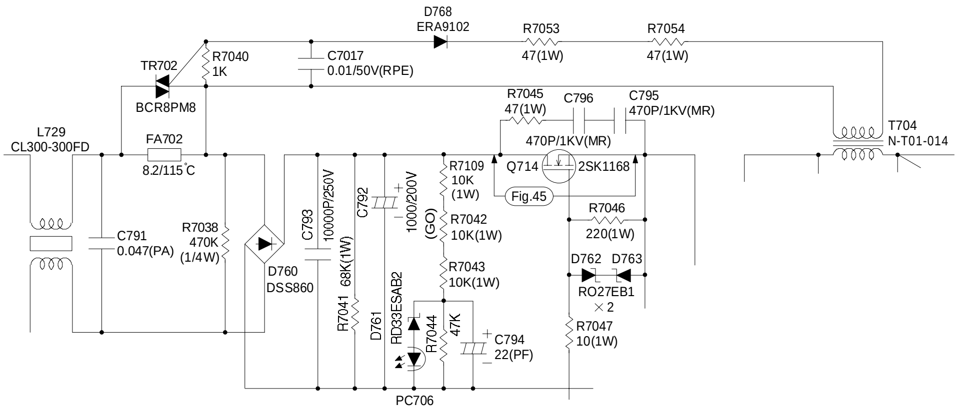


Fig. 33 Rush current limit circuit

c. Rectifying/smoothing circuit

Similarly to the main section, the AC voltage of 50Hz (60Hz) is rectified by the rectifier diode (D760) and smoothed by the smoothing capacitor (C792). The solid line and the dotted line show the path of the charging current to C792.

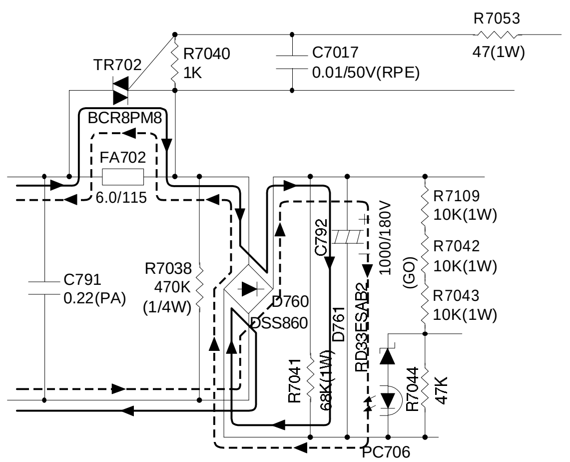


Fig. 34 Rectifying/smoothing circuit

d. Invertor circuit (Chopper regulator circuit)

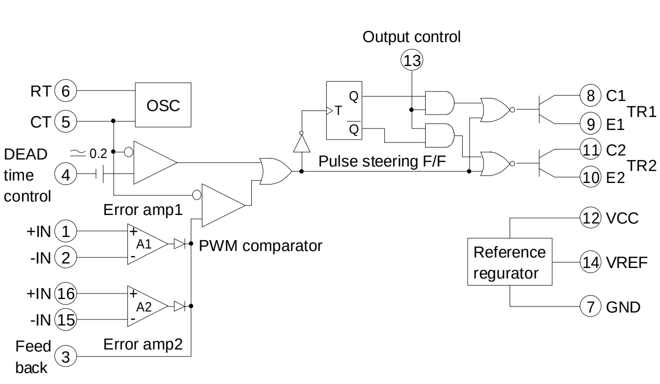
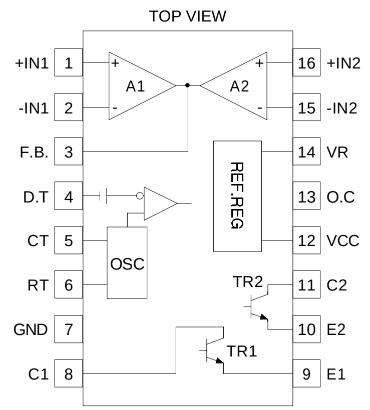


Fig. 35 IC712 block diagram



After rectifying and smoothing the AC power, the copy lamp voltage is stabilized by the voltage-fall type chopper circuit (same as the chopper in the main section).

The switching frequency generates triangle waveforms of about 50KHz by CR connected to IC712 5pin and 6pin.

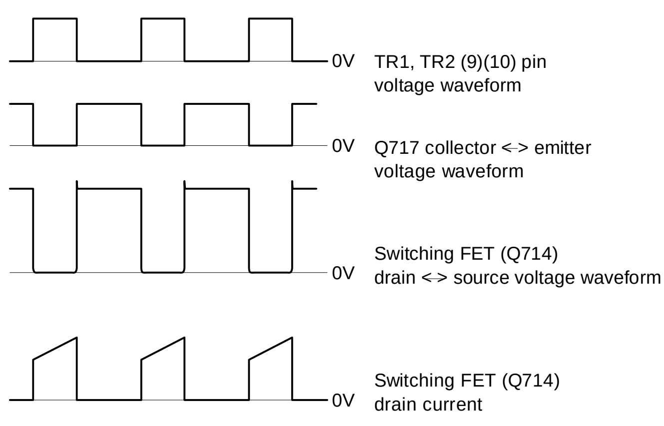


Fig. 36 Switching waveform in each section

e. Overvoltage protection circuit

When an overvoltage is generated in the copy lamp section, it is detected by the overvoltage detection circuit to turn off the power relay (S701) to stop the operation of the copy lamp.

The operation is of the latch system. After removing the overvoltage, supply the AC power to reset.

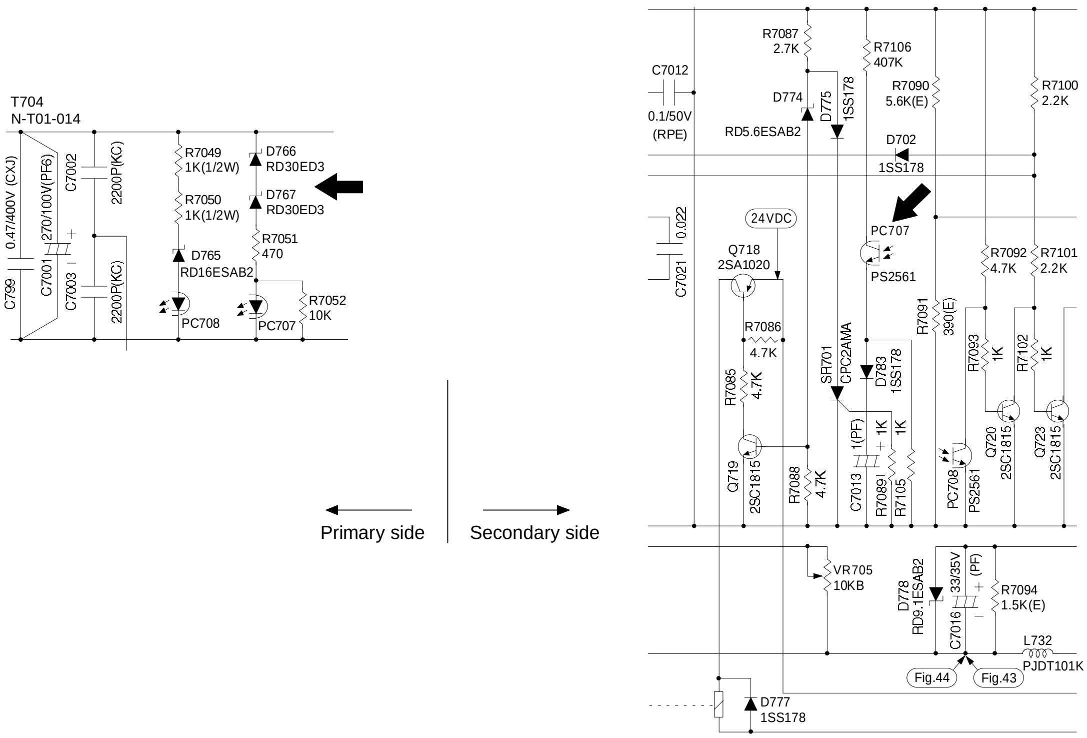


Fig. 37 Overvoltage protection circuit

f. CLCON signal

The CL voltage is varied by the CLCON signal (PWM). The relationship between the CLCON signal and the CL voltage is as shown in the figure below.

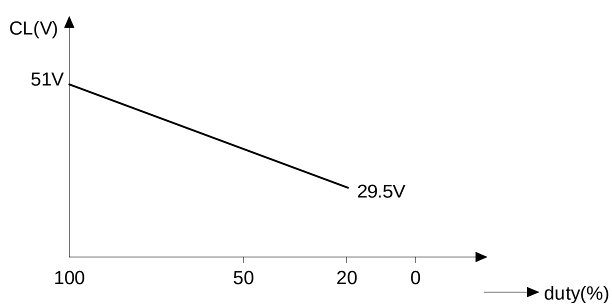
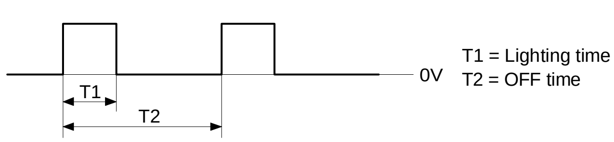


Fig. 38 CL voltage ~ CLCON duty

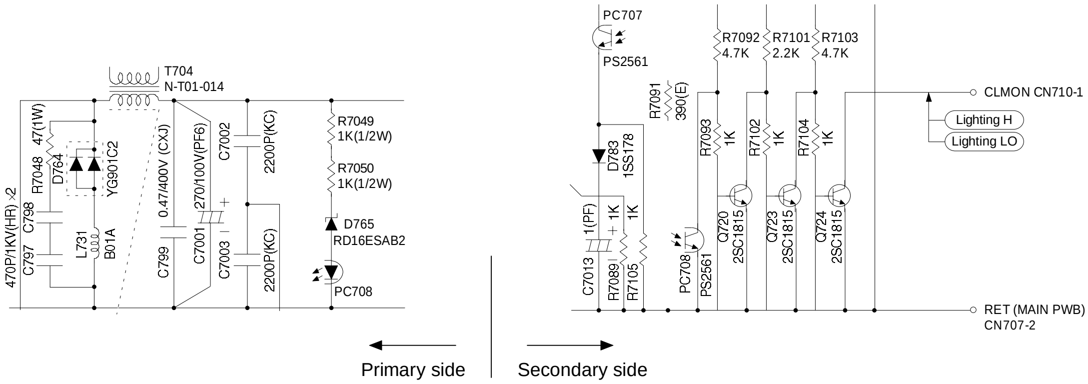


T2 = 819.9µs (1.22KHz)
duty = T1/T2 x 100 (%)

Fig. 39 CLCON signal

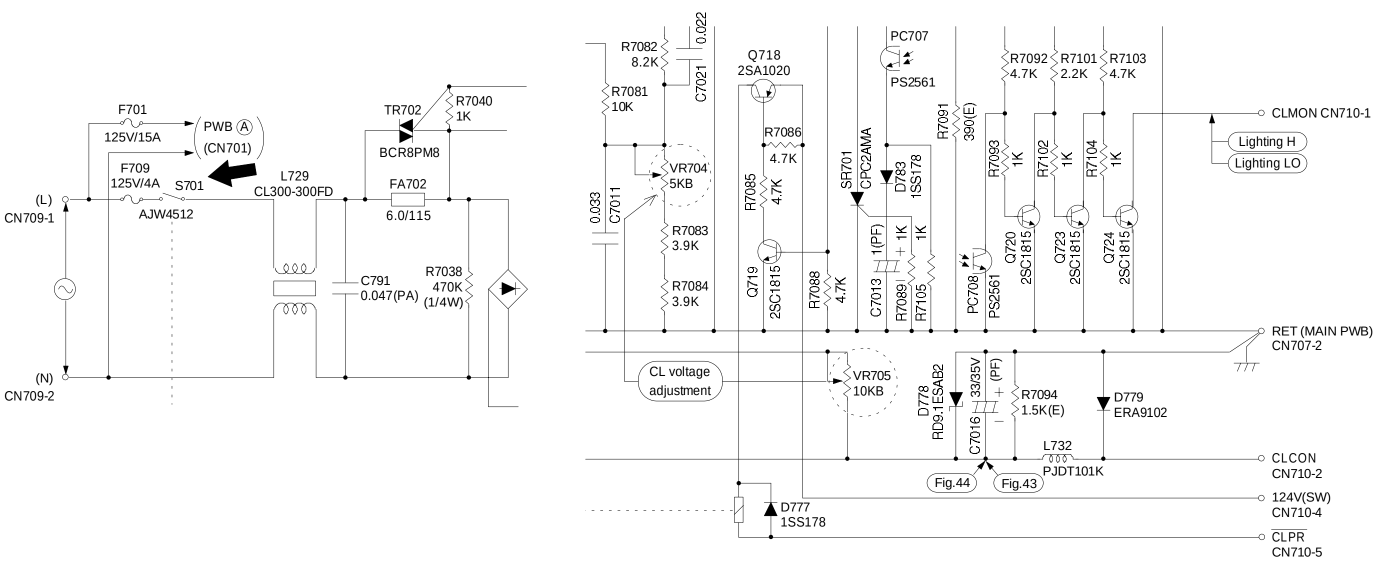
g. CLMON signal

This signal monitors the CL output voltage. ON (lighted) at HIGH, and OFF at LOW.

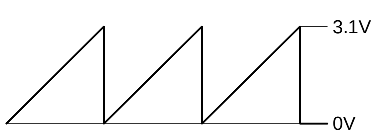


h. $\overline{\text{CLPR}}$ signal

This signal controls the power relay (S701) in the AC input section. ON at HIGH, and OFF at LOW. When the CL voltage becomes an overvoltage, the power relay is turned off even through the CLPR is LOW.



[Waveform of each section]



Condition: Input 100VAC

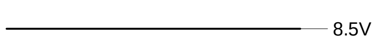


Fig. 42 IC712 ⑤ pin voltage

Fig. 43 C7016 voltage (duty 100%)

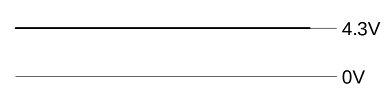


Fig. 44 C7016 voltage (duty 20%)

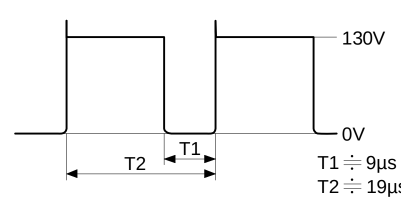


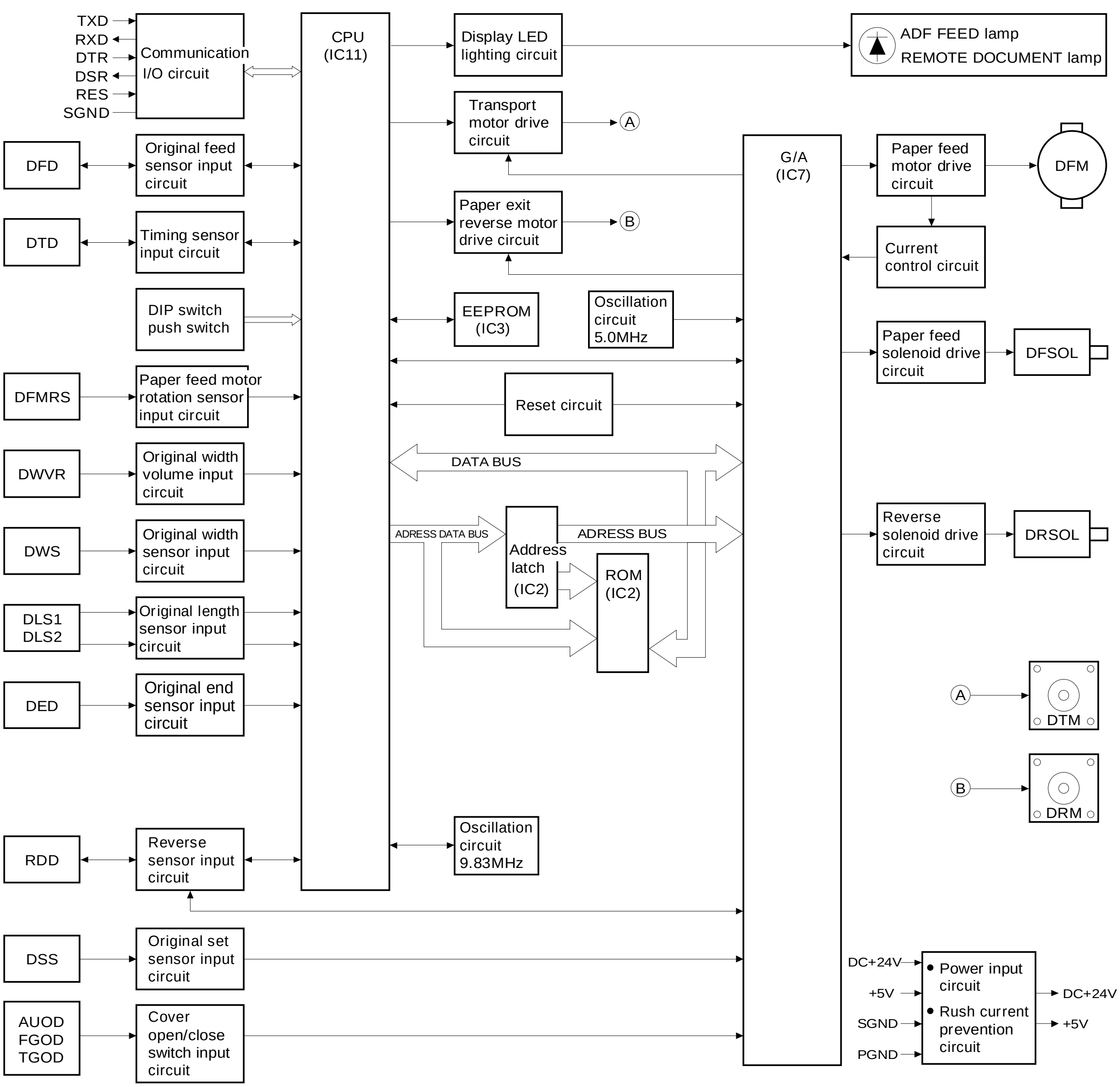
Fig. 45 Q714 drain-source voltage waveform

[10] RADF ELECTRICAL SECTION

1. General

This circuit controls feeding, stopping, and reversing of the document. It is composed of sensors, switches, the circuit which processes signals from the copier PPC, the circuit which drives motors, solenoids, and clutches, the CPU, the G/A and its peripheral circuits.

2. Block diagram



3. Operations

A. Sensor input circuit

[a] Document timing sensor (DTD)

The document timing sensor is a reflection type sensor, and the LED and the photo transistor are integrated into one. Infrared light emitted from the LED is reflected by the mirror on the opposite side, and the reflected light enters the photo transistor to increase the photo current in the photo transistor, detecting "No document."

On the other hand, if there is an document between the LED and the mirror, there is no reflection from the mirror. Therefore the photo current does not increase and the document is detected.

This circuit is also provided with the automatic adjustment function.

The LED cathode is connected to the voltage-current conversion circuit composed of the operation amp (IC13), Q3, and R94. The current value is controlled with the D-A output (analog voltage output) from the CPU. That is, the operation is made so that the CPU D-A output value (IC11-67 pin) is equal to IC13 2 pin input voltage (the voltage drop of LED current by R94).

When, therefore, the D-A output value is changed, the current value is also changed.

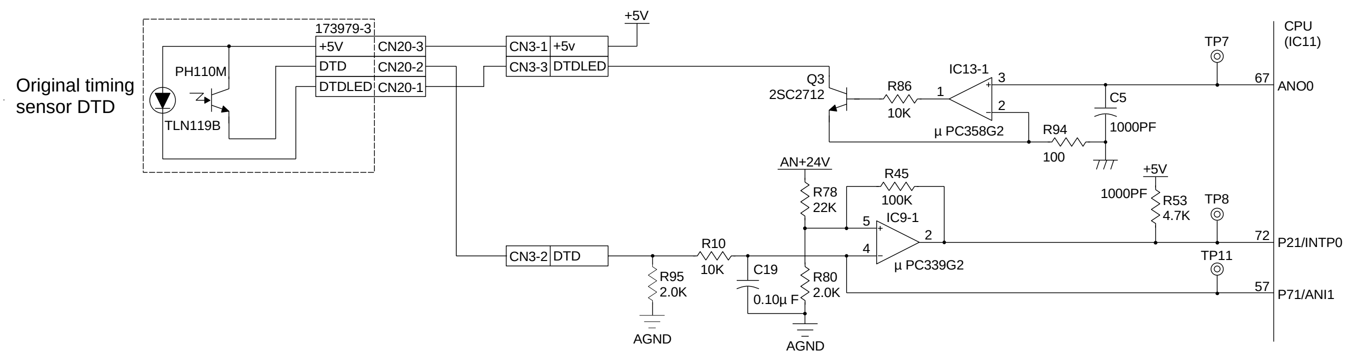
On the other hand, the photo current of the photo transistor is converted into a voltage value by load resistor R95, and is inputted to IC9 4 pin and the CPU 57 pin through the noise filter composed of R10 and C19.

R78, R80, R45, and IC9 form a voltage comparator, which compares the input voltage from the sensor with the threshold voltage (about 2V) generated by dividing +24V with R78 and R80.

When the sensor input voltage exceeds the threshold voltage, the output of IC9 2pin turns LOW, being inputted to the CPU 72 pin as "No document" signal.

The CPU 57 pin is an A-D input pin, which converts an analog voltage into a digital value inside the CPU. Since the sensitivity of a sensor generally varies, it is automatically adjusted with the sensitivity at "No document" as the reference voltage. That is, the sensor voltage at "No document" is A-D inputted to change the D-A output voltage, varying the LED current (LED light intensity) and controlling by the CPU so that the sensor voltage is the specified constant level.

The D-A output value at that time is unique to every machine, and is stored in the EEPROM (IC3).



Original timing sensor input circuit

[b] Document feed sensor (DFD)

The document feed sensor is a reflection type sensor, and the LED and the photo transistor form a pair. Infrared light emitted from the LED is reflected by the mirror on the opposite side, and the reflected light enters the photo transistor to increase the photo current in the photo transistor, detecting "No document."

On the other hand, if there is an document between the LED and the mirror, there is no reflection from the mirror. Therefore the photo current does not increase and the document is detected.

This circuit is also provided with the automatic adjustment function.

The LED cathode is connected to the voltage-current conversion circuit composed of the operation amp (IC13), Q3, and R94. The current value is controlled with the D-A output (analog voltage output) from the CPU. That is, the operation is made so that the CPU D-A output value (IC11-68 pin) is equal to IC13 5 pin input voltage (the voltage drop of LED current by R93).

When, therefore, the D-A output value is changed, the current value is also changed.

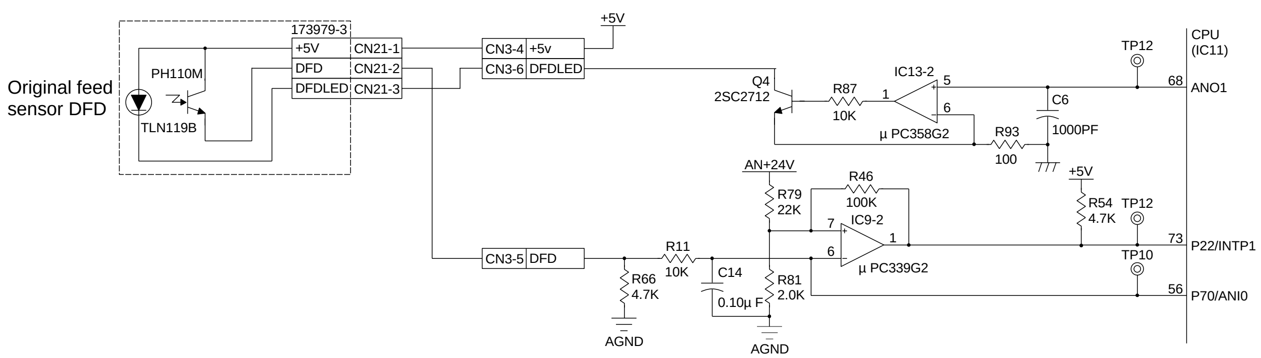
On the other hand, the photo current of the photo transistor is converted into a voltage value by emitter resistor R66, and is inputted to IC9 6 pin and the CPU 56 pin through the noise filter composed of R101and C14.

R79, R81, R46, and IC9 form a voltage comparator, which compares the input voltage from the sensor with the threshold voltage (about 2V) generated by dividing +24V with R79 and R81.

When the sensor input voltage exceeds the threshold voltage, the output of IC9 1pin turns LOW, being inputted to the CPU 73 pin as "No document" signal.

The CPU 56 pin is an A-D input pin, which converts an analog voltage into a digital value inside the CPU. Since the sensitivity of a sensor generally varies, it is automatically adjusted with the sensitivity at "No document" as the reference voltage. That is, the sensor voltage at "No document" is A-D inputted to change the D-A output voltage, varying the LED current (LED light intensity) and controlling by the CPU so that the sensor voltage is the specified constant level.

The D-A output value at that time is unique to every machine, and is stored in the EEPROM (IC3).



Original feed sensor input circuit

[c] Reverse sensor (RDD)

The reverse sensor is a reflection type sensor, and the LED and the photo transistor are integrated into one. Infrared light emitted from the LED is reflected by the mirror on the opposite side, and the reflected light enters the photo transistor to increase the photo current in the photo transistor, detecting "No document."

On the other hand, if there is an document between the LED and the mirror, there is no reflection from the mirror. Therefore the photo current does not increase and the document is detected.

This circuit is also provided with the automatic adjustment function.

The LED cathode is connected to the circuit composed of R107, R108, and Q17. A high level or a low level input is passed to the base of Q17 to vary the LED light quantity.

The base of Q17 is connected to the CPU 49 pin. When the CPU outputs a low level signal, Q17 is turned off and all forward current in the LED flows through R108.

On the contrary, when the CPU outputs a high level signal, Q17 is turned on and the forward current in the LED flows through R108 and R107 in parallel. That is, the forward current in the LED is doubled, increasing the light quantity.

On the other hand, the output voltage of the photo transistor is inputted through the noise filter composed of R32 and C20 to IC9 10 pin.

IC9 and R48 form a voltage comparator, which compares the sensor output voltage inputted to 10 pin and the threshold voltage inputted to 11 pin.

When the sensor output voltage is lower than the threshold voltage, the output at IC9 13 pin turns HIGH and the "document present" signal is inputted to the CPU (IC11) 75 pin.

Since the sensitivity of a sensor generally varies, it is automatically adjusted with the sensitivity at "No document" as the reference voltage. That is, the sensor voltage at "No document" is reduced into 1/3 by R74 and R63 and inputted to the CPU 58 pin.

At that time, the base of Q17 is at LOW level and the light quantity of the LED is kept low. The CPU 58 pin is an A-D input pin, which allows conversion of an analog voltage into a digital voltage in the CPU. When the sensor output voltage inputted to the CPU is in the range of 1V ~ 4.5V, the gate array outputs from 18 pin the PWM signal of the duty corresponding to the voltage inputted to the CPU 58 pin.

The PWM signal is inputted to the integral circuit composed of R31 and C46 and converted into an analog voltage to be inputted to IC14 3 pin.

The converted analog output is the same as the sensor output voltage inputted to the CPU.

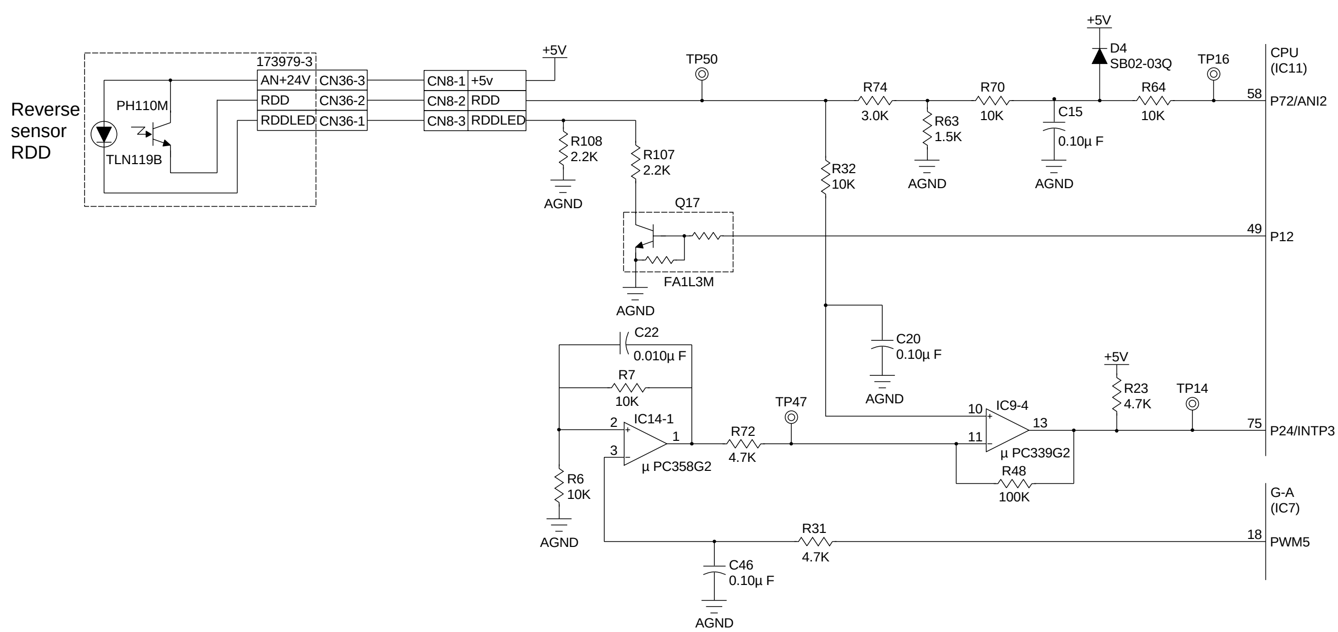
C22, R7, R6, and IC14 form a non-reverse amplifier, which amplifies the analog voltage inputted to IC14 3 pin to be double and outputs from 1 pin.

The output voltage is inputted to IC9 11pin as the threshold voltage, and compared with the sensor output voltage. That is, the threshold value is set to 2/3 of the HIGH level of each sensor output. When the sensor output voltage inputted to the CPU 58 pin is lower than 1V, the gate array 18 pin outputs a HIGH level signal to increase light quantity of the LED. If the output voltage is increased to the range of 1V ~ 4.5V by this, the threshold value setting similar to the above is performed.

If the sensor output voltage remains lower than 1V even though the light quantity of the LED is increased, it is judged as a sensor error.

If the sensor output voltage inputted to the CPU 58 pin is greater than 4.5V, the threshold value cannot be set and it is judged as a sensor error.

The set threshold voltage and the logic of CPU 49 pin when setting are unique to each machine and stored in the EEPROM (IC3).

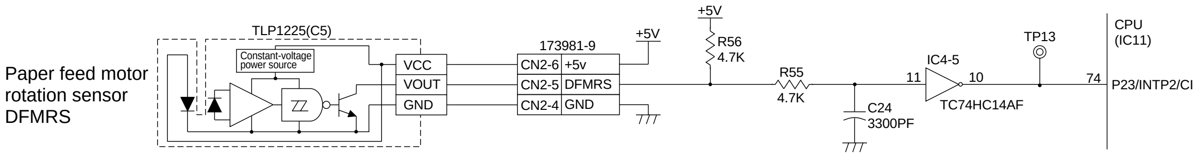


Reverse sensor input circuit

[d] Paper feed motor rotation sensor (DFMRS)

This sensor senses rotation of the paper feed motor, and is composed of the photo interrupter built in the amplifier and the slit disc attached to the motor shaft. The pulse signals corresponding to the motor speed are obtained. the motor rotation speed is sensed from the frequency of the pulse signals, and the motor rotation amount is sensed by counting the pulse numbers.

The input section of signals is a noise filter composed of R55, C24, and Schmidt trigger invertor, which processes signals.



Paper feed motor rotation sensor input circuit

[e] Tray document size sensor, volume circuit

This circuit senses the document size on the tray, and its sensor section is built in the tray.

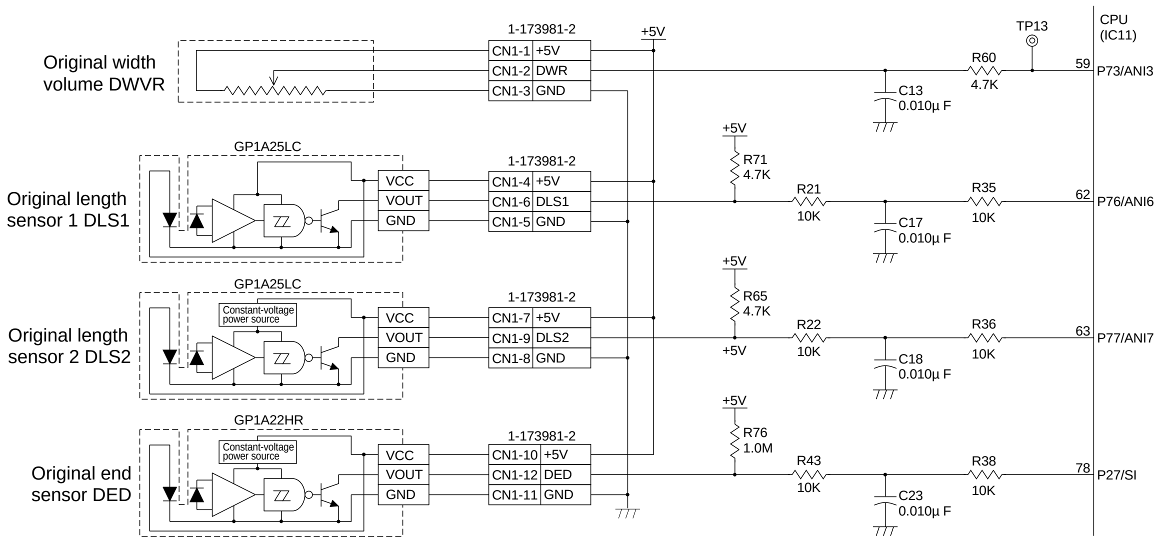
The document width is sensed by the slide volume (DWVR), and the document length is sensed by the two photo interrupters (DLS1, DLS2). (Only DSL1 for AB series)

The DWVR varies the resistance of the variable resistor with the lever attached to the document guide, and the variation is sensed as the voltage value.

The signal is analog-inputted to the CPU A-D input pin (IC11 59 pin). On the other hand, DSL1 and DSL2 use the photo interrupter which is integrated with the light emitting diode and the photo transistor. When there is an document, the lever-type actuator interrupts the optical path. The signal is inputted through the noise filter to the CPU.

DSL1: IC11 62 pin
DSL2: IC11 63 pin

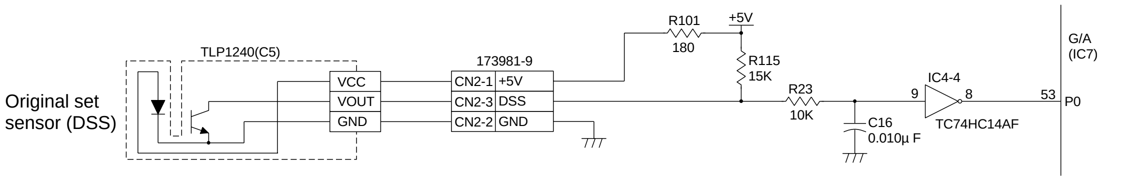
The document end sensor (DED) which senses the third document also uses a photo interrupter, and the signal is inputted through the noise filter to the CPU (IC11 78 pin).



Tray original size sensor circuit

[f] Document set sensor (DSS)

The DSS uses a photo interrupter which is integrated with a light emitting diode and a photo transistor. The signal is passed through the noise filter composed of R23, C16, and Schmidt trigger invertor (IC4) to the gate array (IC7 53 pin), then passed through the data bus to the CPU.



Original set sensor input circuit

[g] Document width sensor (DWS)

The DWS uses a photo interrupter which is integrated with a light emitting diode and a photo transistor. When there is an document, the lever-type actuator interrupts the optical path.

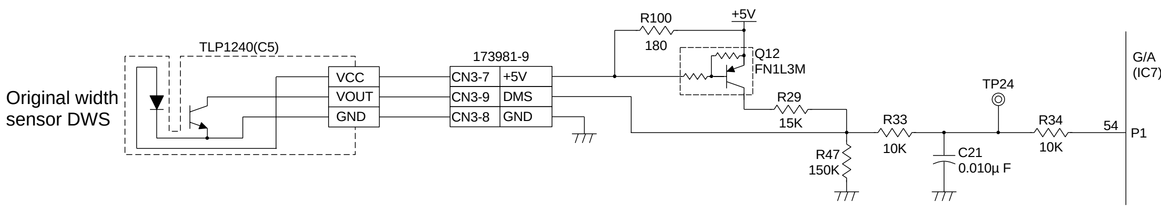
The circuit composed of Q12, R100, R29, and R47 is the connector disconnection sense circuit. When the connectors are not disconnected, the base voltage (5V) of Q12 is divided by R100 and the LED of the photo interrupter to be about 1.2V, conducting the transistor.

At that time, the photo transistor is turned off under "paper empty" state, and the collector current of Q12 flows into R47.

Therefore, the signal DWS turns HIGH by the value (about 4.5V) obtained by dividing +5V with R49 and R47. When in "Paper present," the photo interrupter turns ON and the collector current of Q12 flows into the photo interrupter. As a result, signal DWS turns LOW.

On the other hand, when a connector is disconnected, the base voltage of Q12 becomes +5V, turning off the transistor. Therefore, signal DWS turns LOW and it is judged as "Paper present."

Signals are inputted through the noise filter composed of R33 and C21 to the gate array (IC7 54 pin).



Original width sensor input circuit

[h] Open/close switch (AUOD, FGOD, TGOD) input circuit

This circuit senses open/close of the ADF unit, the paper feed guide, and the reverse guide, and is connected with three microswitches. Any switch is closed when its open/close section is closed.

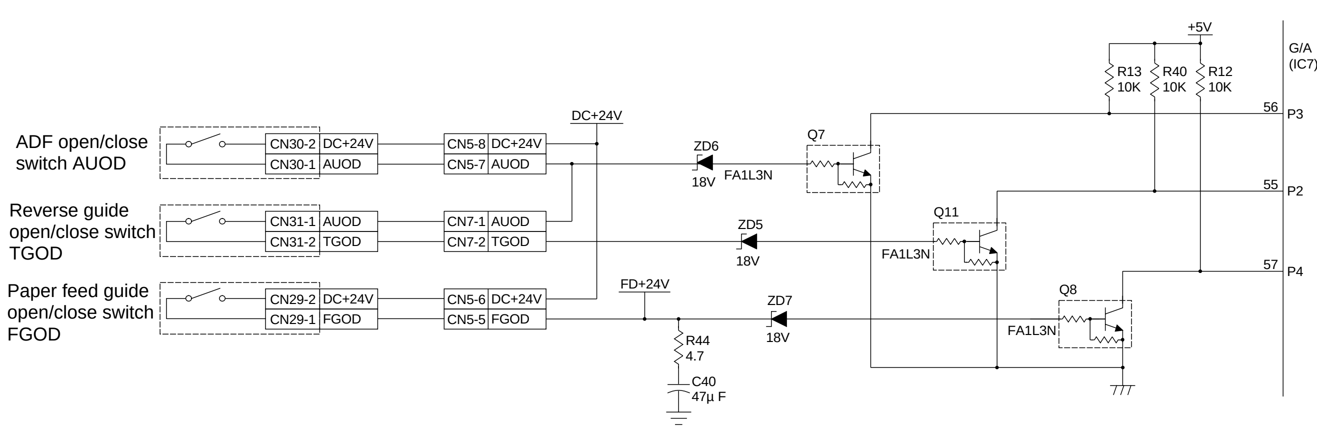
The FGOD directly opens/closes the power to the paper feed motor and the paper feed solenoid. If the FGOD is not closed, the power is not supplied to the paper feed motor and the paper feed solenoid.

The AUOD and the TGOD are connected in series to +24V, and directly close the power to the drive sections except for the paper feed motor and the paper feed solenoid. That is, the power is supplied to the drive sections except for the paper feed motor and the paper feed solenoid only when the two switches (AUOD, TGOD) are closed.

When the paper feed guide open/close switch is turned on, +24V is applied to the cathode of ZD7, supplying the base current to Q8, conducting Q8, supplying an open/close signal (a close signal in this case) to IC7 57 pin.

Operations in the other open/close switch circuits are the same as above, and each open/close signal is inputted to IC7.

R44 and C40 form a snubber circuit which absorbs an induced voltage generated when the open/close switch is opened during rotation of the DC motor.



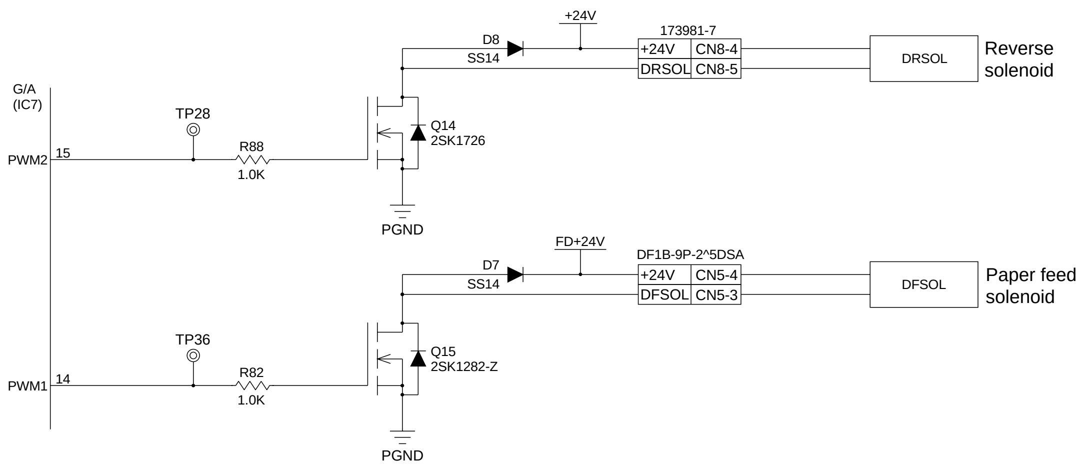
Open/close switch input circuit

B. Solenoid drive circuit

[a] Paper feed solenoid (DFSOL), reverse solenoid (DRSOL) drive circuit

This circuit drives the weight plate which presses the bundle of documents on the tray, the paper feed solenoid which drives the paper feed section shutter, and the reverse solenoid which drives the reverse guide to lead an document to the reverse path when reversing. The basic composition is the same. The drive signal (ON at HIGH) from the gate array is inputted to the gate of FET (Q14, Q15).

The ON duty of the drive signal can be varied from 0 to 100% (255 steps). The frequency, however, is 20kHz.



Solenoid drive circuit

C. Other circuit

[a] EEPROM (IC3) circuit

This circuit serves as a memory to save the sensitivity data of the reflection type sensors, the adjustment values such as the document set position on the document table, and the counter values such as the number of documents passed. Data communication with the CPU (IC11) is performed with the 3-wire serial interface.

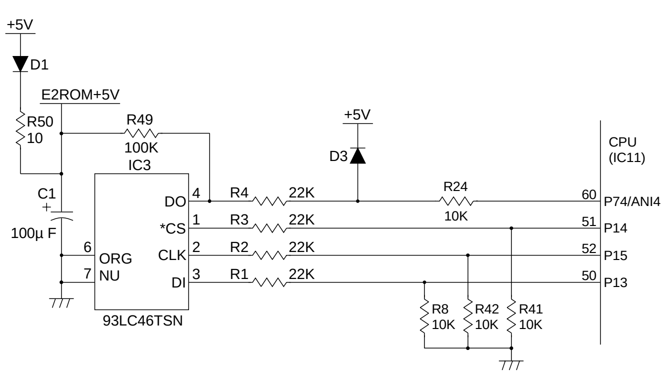
The saved data are maintained even when the power is turned off.

IC3 1 pin is the chip select pin, which is driven to HIGH when data communication is performed.

2 pin is the serial lock pin, and the serial data are transmitted in synchronization with the clock inputted to this pin.

3 pin is the input pin of serial data from the CPU. 4 pin is the output pin of serial data from IC3.

D1, R50, and C1 form a circuit which keeps the power of IC3 at a constant level even when a sudden power drop occurs during data writing.



EEPROM circuit

[b] Reset circuit

This circuit generates reset signals for the CPU and the external G/A, and is composed of IC6 and its peripheral circuits.

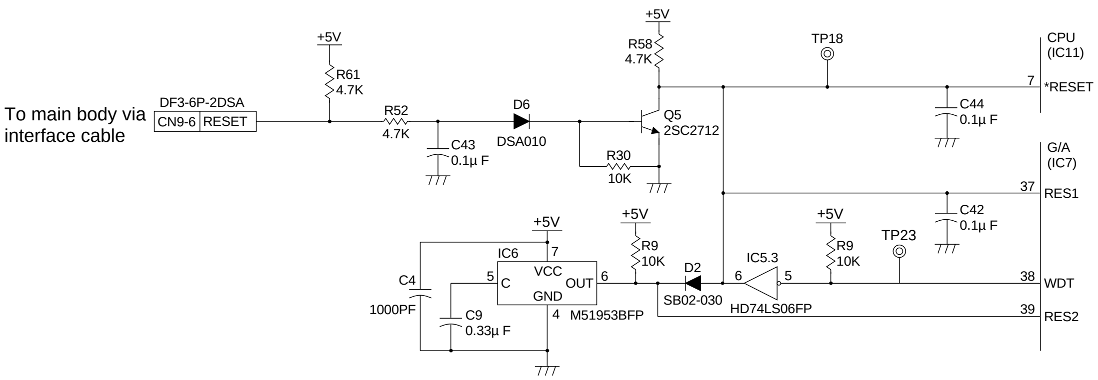
IC6 is provided with the reset function activated when the power is turned on and when the power falls below +5V.

The reset state is maintained until a certain time passes from when the power voltage reaches about 4.3V after supplying the power. The reset maintaining time depends on the capacity of C9.

This circuit is also provided with the watch-dog timer function.

The watch-dog timer is built in the G/A (IC7) and is operated when RES2 turns HIGH. It monitors hung-up or other abnormalities of the CPU. RES2 is reset for the watch-dog timer in the G/A, and is separated from the CPU and RES1 of the G/A by D2. Therefore, the CPU reset and the G/A RES1 do not turn HIGH prior to RES2.

For monitoring, data (initial values) are written from the CPU to the G/A once for every 5ms. (Resetting to the initial values every 5ms.) The data are counted down inside the G/A. Since the values are reset to the initial values every 5ms, the count normally does not fall to zero. If, however, a hung-up of the CPU occurs, the data are not reset to the initial values, and the counter becomes zero. At that time, resetting is performed from the G/A to the CPU and the G/A (RES1), and retry is performed until the CPU is resumed.



Reset circuit

[c] Paper feed motor (DFM) drive circuit

This circuit controls the paper feed motor rotation and stop and the rotating direction. It is composed of the G/A (IC7) and the exclusive hybrid IC (IC10), etc.

The motor rotation, stop, and rotating direction are controlled by the combination of binary logics inputted to the G/A through the data bus from the CPU.

This provides control signals to the G/A 65 ~ 68 pins.

The G/A 65 pin and 66 pin are for the PWM output for speed control. (Normal rotation, 65 pin; reverse rotation, 66 pin)

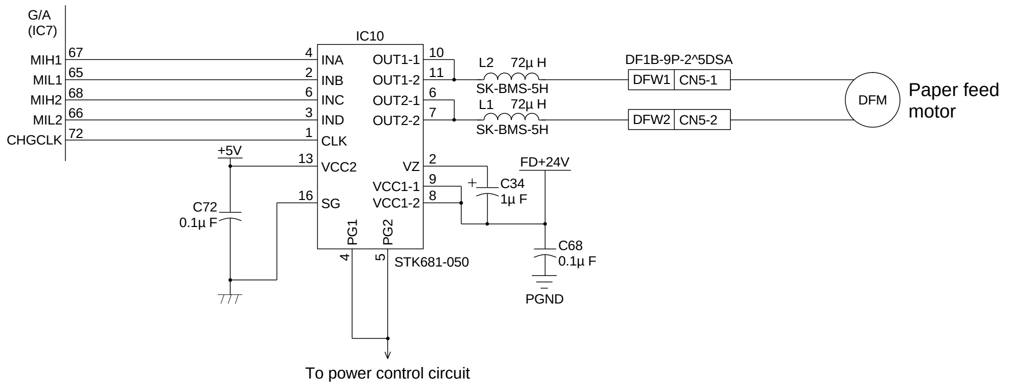
These signals are inputted to IC10.

IC 10 is a hybrid IC including 4 power MOSFET's, and drives the motor by taking the G/A output 65 ~ 68 pins.

The motor operates as follows by the combination of 25 ~ 28 pins.

—	65	66	67	68
Before start	0	0	0	0
CCW	0	PWM	1	0
CW	PWM	0	0	1
Brake	0	0	1	1

In the brake mode, the both terminals of the motor are shorted, generating a great braking torque to stop the motor.



Paper feed motor drive circuit

[d] Transport motor (DTM) drive circuit

This circuit controls the transport motor rotation/stop, the rotating direction, and the motor current. It is composed of the CPU (IC11), the constant current chopper system driver IC (IC8), and the G/A (IC7).

The motor rotating speed and the rotating direction are controlled with the stepping motor drive excitement pattern signals from the CPU (12 ~ 15 pins).

The PWM (20KHz) signal from the G/A (17 pin) is divided and integrated by R113, bR116, and C39 to be converted into a constant voltage, which is inputted to IC8 (9 pin, 11 pin) to set the motor current value.

By varying the PWM signal duty, a desired motor current value can be obtained.

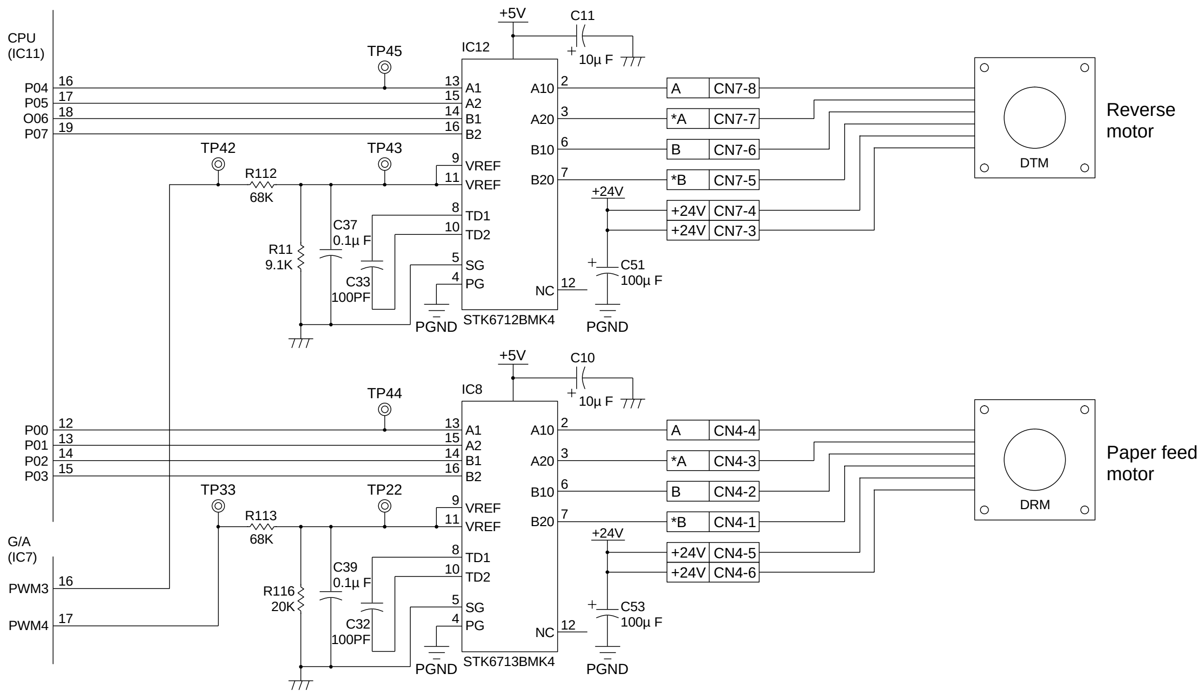
[e] Reverse motor (DRM) drive circuit

This circuit controls the reverse motor rotation/stop, the rotating direction, and the motor current, and is composed of the CPU (IC11), the constant-current chopper system driver IC (IC12), and the G/A (IC7).

The motor rotating speed and the rotating direction are controlled with the stepping motor drive excitement pattern signals from the CPU (16 ~ 19 pins).

The PWM (20KHz) signal from the G/A (16 pin) is divided and integrated by R112, bR114, and C37 to be converted into a constant voltage, which is inputted to IC12 (9 pin, 11 pin) to set the motor current value.

By varying the PWM signal duty, a desired motor current value can be obtained.



Transport motor/reverse motor drive circuit

[f] Paper feed motor (DFM) current limiting circuit

This circuit limits the motor start current to a constant level, and is composed of the resistor for detection of the current value and the voltage comparator.

The negative voltage side of the paper feed motor is connected to the;pickup resistor composed of R97, R98, and R99, which converts the current flowing in the driver circuit into a voltage value.

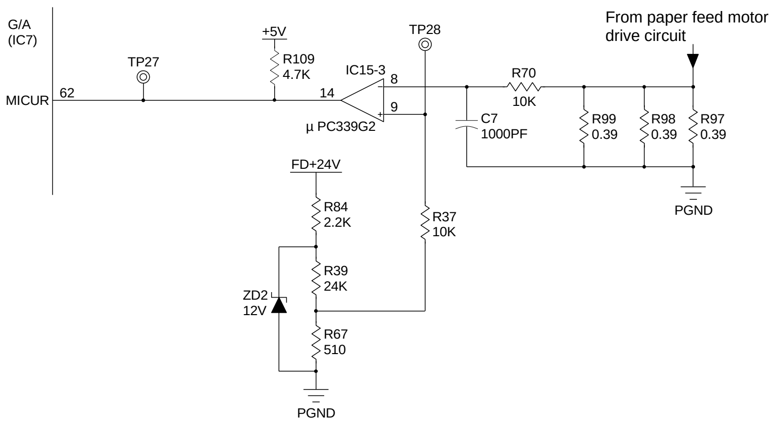
The converted voltage value is compared with the reference voltage by IC9 comparator.

The reference voltage is obtained by dividing the zenor voltage generated from R84 and ZD2 with R39 and R67. It is about 0.3V. When the converted voltage value exceeds the reference voltage (about 2.8A in the current value), IC9 14 pin turns LOW and the signal is inputted to the G/A 62 pin, interrupting +24V supply to the motor. As a result, the current value is limited.

When the converted value falls below the reference value, +24V is supplied again to resume conduction to the motor.

Since the operating current of this circuit is considerably great,

it operates only when starting the motor and does not operate in the normal state.



Paper feed motor current control circuit

[g] Rush current limiting circuit

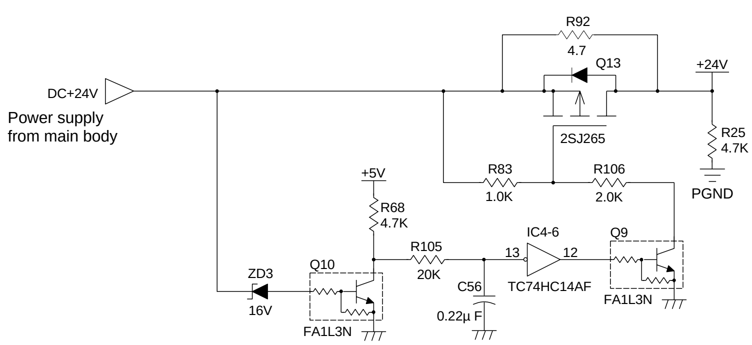
This circuit limits a rush current which flows into the current generation capacitors (C53, C54) in the transport motor (DTM)/reverse motor (DRM) drive circuit, and is composed of the limiting resistor and the FET which allows to flow a constant current.

After closing the ADF open/close switch (AUOD) and the reverse guide open/close switch (TGOD) and until the cathode voltage of ZD3 reaches 16V, the base current is not supplied to Q10, which is kept OFF, driving IC4 3 pin HIGH.

At that time, the base current of Q9 is not supplied to turn off Q9, turning off Q3, flowing a current through R92.

On the other hand, when the cathode voltage of ZD3 exceeds 16V, the base current of Q10 flows to conduct the transistor, turning on Q13. As a result, the current which was flowing through R92 flows through Q13 to cancel current limiting.

R25 is the discharging resistor which discharges electric charge in C53 and C54 when the ADF open/close switch (AUOD) or the reverse guide open/close switch (TGOD) is opened.



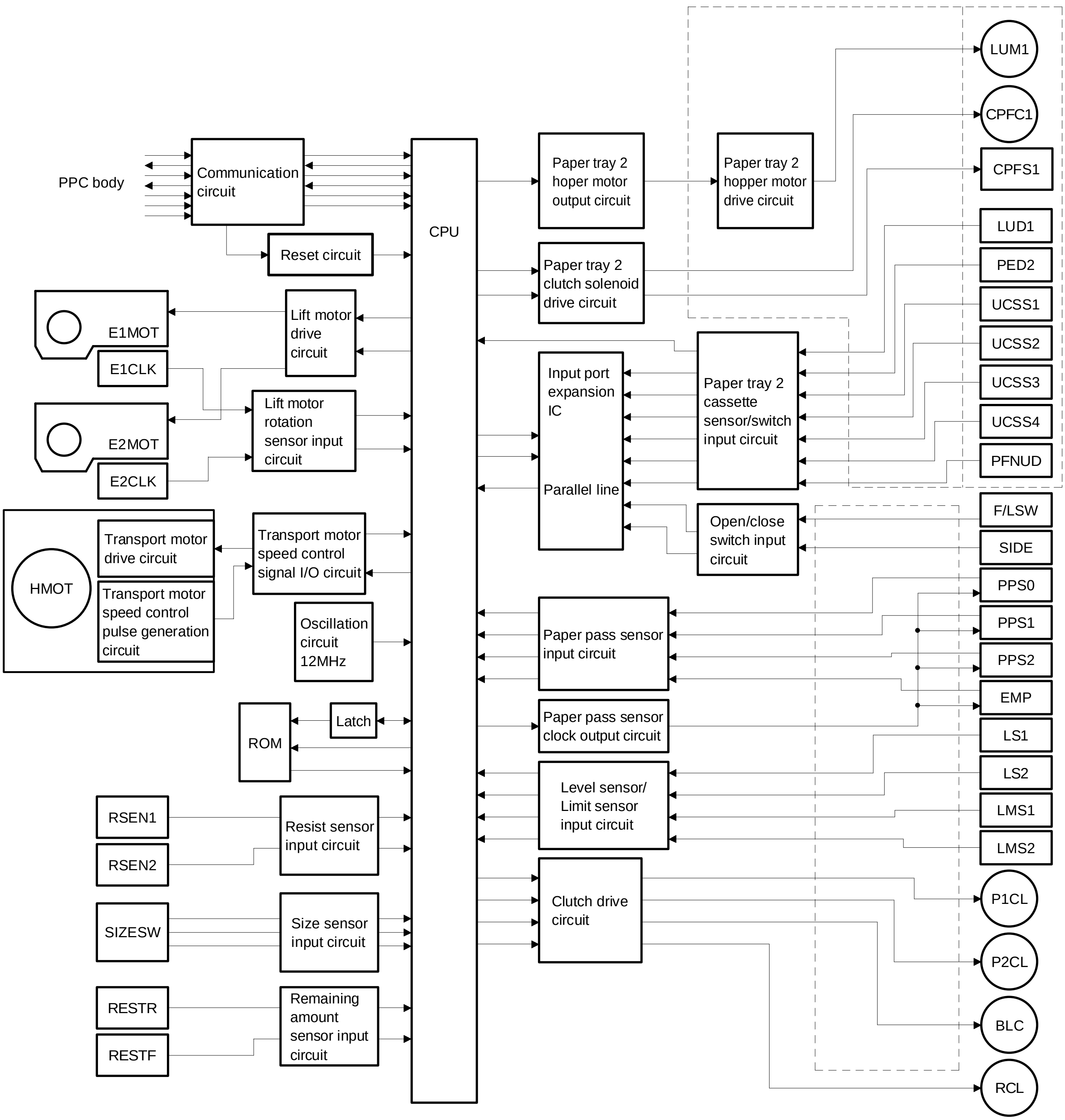
Rush current prevention circuit

[11] DESK UNIT ELECTRICAL SECTION

1. Outline

This circuit controls paper feed to the copier body, and is composed of sensors, switches, the circuit to interface with the copier, the circuit to drive motors, clutches, and solenoids, the CPU, and its peripheral circuits.

2. Block diagram



3. Operational descriptions

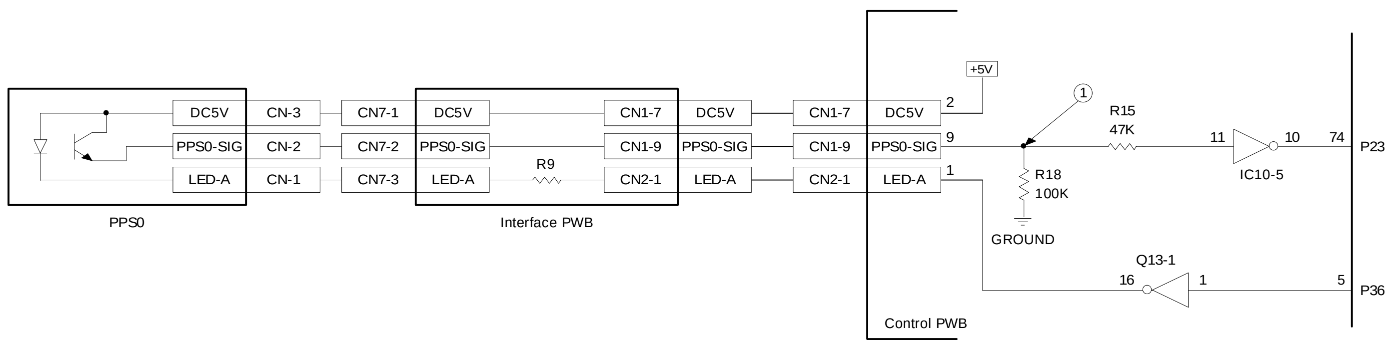
(1) Sensors/detectors input circuit

A. Paper pass sensors (PPS0 ~ PPS2, EMP) input circuit

The paper pass sensors are positioned in the paper transport path and used to detect paper pass. They are reflection type sensors. A sensors is composed of an LED and a photo transistor. Infrared light radiated from the LED is reflected by the paper and passed to the photo transistor, increasing the photo current in the photo transistor to detect paper pass/reach.

Paper pass sensors 0, 1, and 2 and the empty sensor are of the same circuit composition. In the following, paper pass sensor 0 (PPS0) is described.

The LED in the sensor is pulse-lighted. The pulse is generated by the CPU timer, and open-collector-outputted by Q13.1. R9 is the current limit resistor of the LED. When there is the paper just below the sensor, the pulse-lighted infrared light is reflected and passed to the photo transistor. Consequently the photo current in the photo transistor increases and flows through R18. As a result, the voltage at section ① is varied in proportion to the greatness of the incident light. IC10.5 converts this voltage into the digital signals at the threshold voltage (about 3V). When the input voltage of IC10.5 is lower than the threshold voltage, it is judged as paper empty; when greater than the threshold voltage, judged as paper present. Because it is reversed by IC10, when the CPU input is LOW (0V), paper present; and when HIGH (5V), paper empty. The input signal is inputted in the pulse state because the LED is pulse-lighted. The CPU takes this signal in synchronization with the ON/OFF timing of the LED.



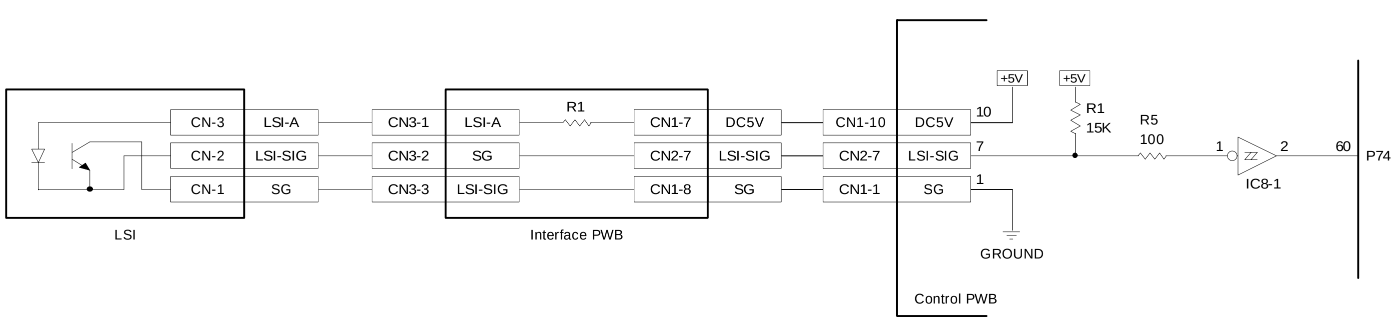
PPS0 input circuit

B. Level sensor/limit sensor (LS1, 2, LMS1, 2) input circuit

To lift the paper in the paper tray 3 to the proper height, the lift up motor is rotated to lift the bundle of paper. At that time, the level sensor (photo interrupter) detects the paper level and the limit sensor detects the upper limit of the lift up operation. The shield plate provided at the pickup roller which is in contact with the paper surface operates in synchronization with the up-down movement of the paper. The position of the shield plate is detected by the photo interrupter. There are two sets of the lift up mechanism, each of which has the level sensor and the limit sensor. The limit sensor controls stop of the lift up motor as well as that the CPU detects the upper limit. (For details, refer to the descriptions on the lift up motor drive circuit.)

The level sensor and the limit sensor are of the same circuit composition. In the following, level sensor 1 (LS1) is described.

The photo interrupter is composed of the LED and the photo transistor (open-collector output). The LED is always lighted by the current limited by R1 in the interface PWB. When the shield plate enters the slit in the interrupter, infrared light from the LED is shielded to turn off the photo transistor (output high impedance). At that time, the LSI signal is driven HIGH (5V) by R1 in the control PWB. When the shield plate is not fitting with the slit, the photo transistor turns on to drive the LS1 LOW (0V). R5 is the input protection resistor of the IC8 1pin. The IC8.1 rectified the waveform of the input signal. Besides, waveform rectification is made only for level sensors 1 and 2, and the signals of limit sensors 1 and 2 are directly inputted to the CPU.



LS1 input circuit

C. Lift motor rotation sensor (E1CLK, E2CLK), remaining amount sensor (RESTR,F), side sensor input circuit

The lift motor rotation sensor senses rotation of the lift motor, and it is composed of the slit disc attached to the rotating shaft of the lift motor and the photo interrupter. When the motor rotates, pulse signals are provided by the sensor. The remaining amount sensor senses the remaining amount of paper in the paper tray 3, and is composed of the photo interrupter and the shield plate provided with the mechanism which operates with the height of the lifter plate of the paper tray 3. The table below shows the truth table of the remaining amount sensor. The side sensor senses open/close of the cover which removes paper jams in the paper transport path.

The circuit compositions of the rotation sensor, the remaining amount sensor, and the side sensor are the same as that of the limit sensor as shown in (b).

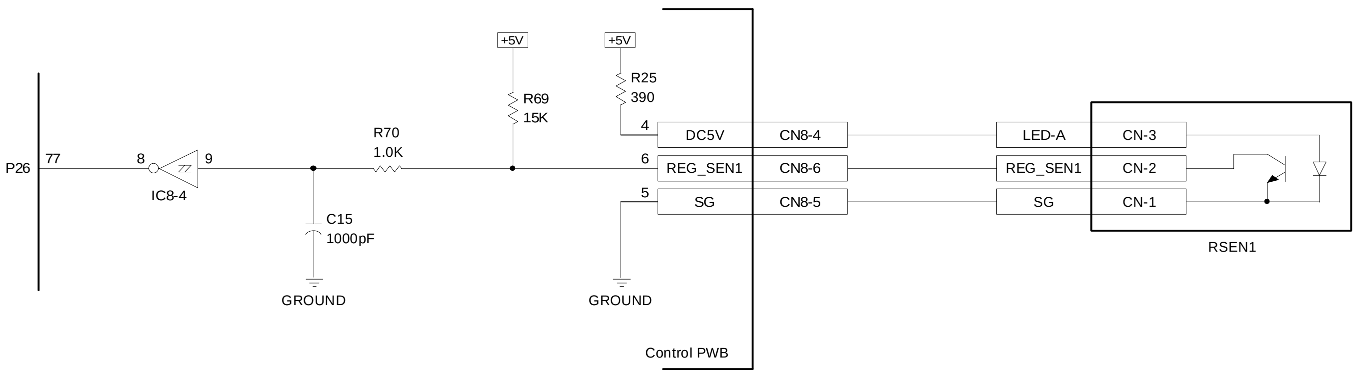
Remaining amount sensor

	Paper remaining amount: 0 ~ 750 sheets	Paper remaining amount: 750 ~ 1500 sheets
REST1, 2	Shield plate ON	Shield plate OFF
	Signal level LO (0V)	Signal level HIGH (5V)

D. Resist sensor (RSEN1, 2) input circuit

The resist sensor is the photo transistor positioned in front of the roller which is in the transport path of paper discharged from the paper tray 3 and the paper tray 2, and is provided with the lever. The transported paper pushes the lever to move it off the sensor slit, and the paper arrival is detected. RSEN1 and TSEN2 are of the same circuit composition. The following description is made on RSEN1.

The photo interrupter is composed of the LED and the photo transistor (open-collector output). A current limited by R25 flows through the LED, which is always lighted. When the lever enters the photo interrupter slit, the infrared light from the LED is shielded to turn off the photo transistor (output high impedance). At that time, the signal of RSEN1 becomes HIGH (5V). When the lever is off the slit, the photo transistor is turned on to drive the signal of RSEN1 LOW (0V). R70 and C15 form a noise filter. IC8.4 rectifies the input waveform.



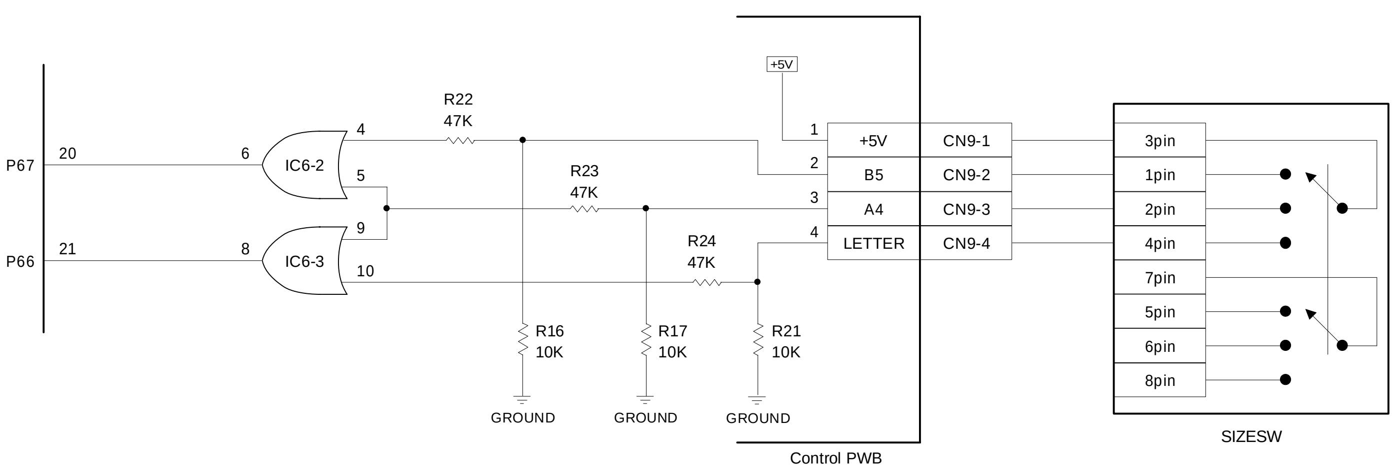
SEN1 input circuit

E. Size switch (SIZESW) input circuit

This is a 3-contact slide switch to switch the paper size (A4, B5, LTR) of the paper tray 3, and is attached to the frame on the left side of the front. The signals are from three lines, and they are HIGH (5V) when ON. The signals of three lines are converted into 2bit by IC6.2, 3. R16, 17, and 21 are pull-down resistors and R22, R23, and R24 are the input protection resistors for IC6.

The truth table is shown in the table below.

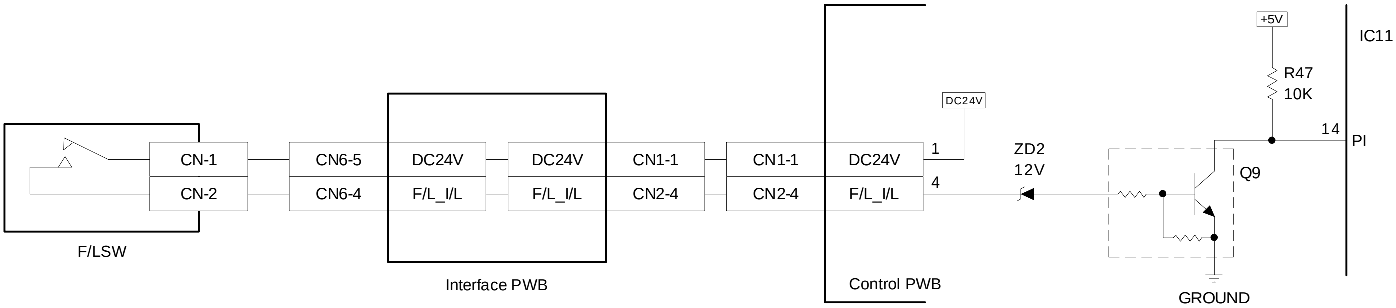
	P67	P66	CN9-2	CN9-3	CN9-4
B5	Hi	Lo	Hi	Lo	Lo
A4	Hi	Hi	Lo	Hi	Lo
Letter	Lo	Hi	Lo	Lo	Hi



SIZES input circuit

F. Open/close switch (F/LSW) input circuit

This circuit is composed of the microswitch which detects open/close of the paper tray 3 and the mechanism to press the switch. When the tray is closed, the switch is turned on. When the tray is opened, the switch is turned off. When the switch is turned on, +24V is applied to the cathode of ZD2 to supply current to the base of Q9, turning on Q9 and driving F/LSW signal LOW (0V).



F/LSW input circuit

G. Paper tray 2 sensor, switch input circuit (UCSS1 ~ 4, LUD1, PED2, PFNUD) and input port expansion IC (IC11)

The paper size select switches (UCSS1 ~ 4) detect the size of paper in the paper tray 2. The paper surface sensor (LUD1) is the photo interrupter which forms the signal to control the hopper motor which lifts paper to the feeding level. The sensor (PED2) is the photo interrupter which detects presence of paper. They are composed of the lever and the photo interrupter. These sensors and switches are positioned in the paper tray 2. The pull-up resistor is used to determine the signal logic, and the resistor connected in series is for protection of the IC11.

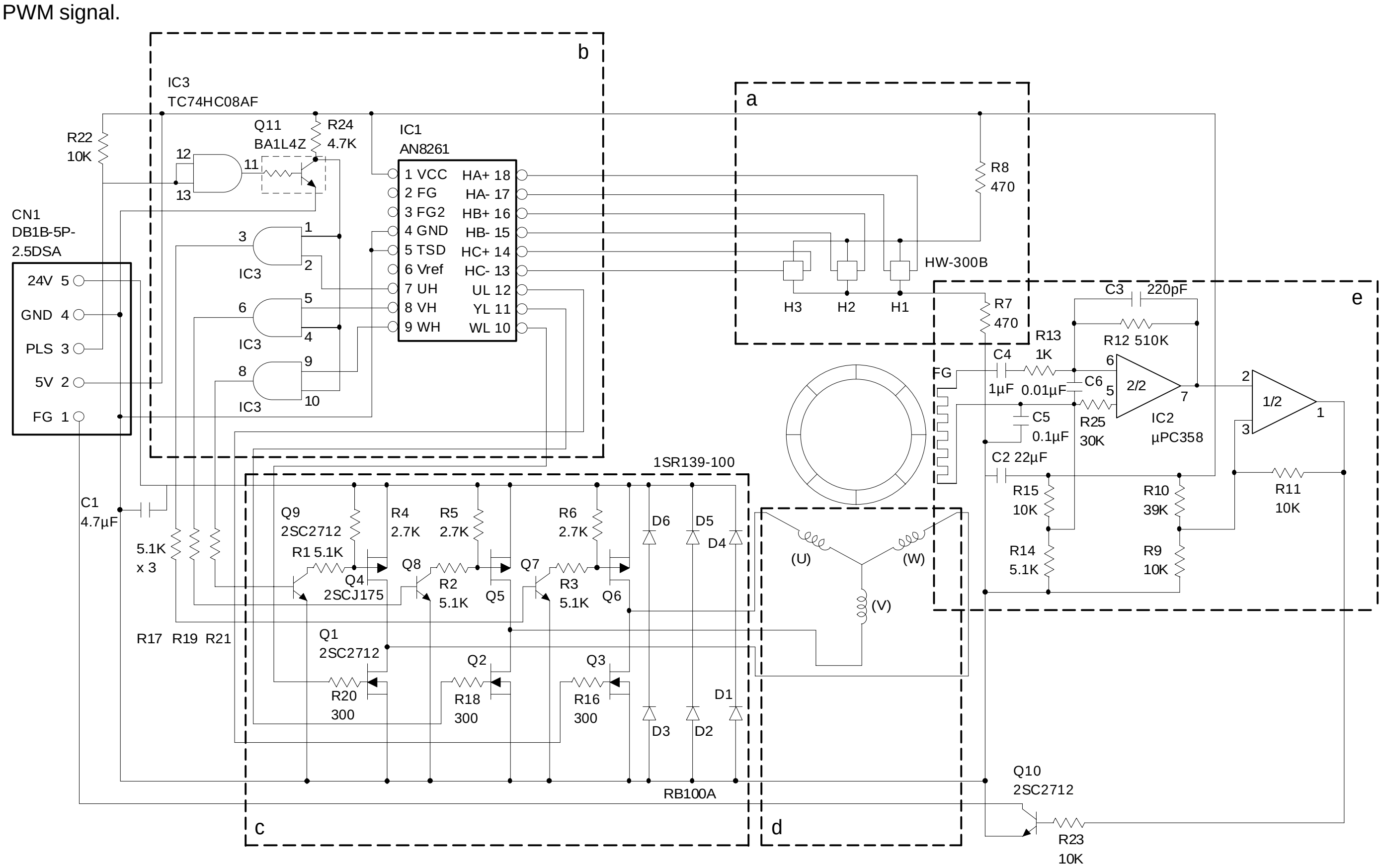
These signals (excluding PFNUD) and the side sensor (SIDE) and the desk open/close sensor (F/LSW) are taken into the IC11 input port. The IC11 converts parallel input signals into serial signals and outputs them in synchronization with CLK. The CPU P32 outputs CLK to the IC11 CLK input pin.

The IC11 latches the parallel input signal at falling of the S/L pin and outputs signals of sensors from the 0h pin in synchronization with CLK. The serial signal is taken into the CPU input pin and used as a sensor signal in the CPU.

(2) Drive system control circuit

A. Paper transport motor speed control circuit (HMOT)

This circuit controls the DC brushless motor which transports paper, and is composed of the pulse generating circuit which allows the CPU to recognize the motor speed and the motor drive circuit which drives the motor by the PWM output according to the pulse (PLS). The motor is composed of the PWB and the rotor. The PWB is provided with the pulse (PLS) generating circuit and the drive circuit. The PWM output is supplied from the CPU. The interface between the CPU PWB and the motor PWB is performed with the powers (24V, 5V), GND, the PLS signal, and the PWM signal.



Motor drive circuit

a. Coil select sensor

H1, 2, 3 are the magnetism sensitive elements (Hall element) used to determine the polarity of the main flux generated when the rotor rotates, producing the coil conduction select signal.

b. Coil select control circuit

The coil select signal (weak analog value around 2.5V)produced by H1, 2, 3 is converted into the HIGH/LOW level judgement signal in the IC1. The table below shows the logic diagram of IC1.

Code		Pin No.	1	2	3	4	5	6
Input	HA+	18	H	H	L	L	L	L
	HA–	17	L	L	H	H	H	L
	HB+	16	L	H	H	L	L	L
	HB–	15	H	L	L	L	H	H
	HC+	14	L	L	L	H	H	H
	HC–	13	H	H	H	L	L	L
Output	UH	7	L	L	H	H	L	L
	VH	8	L	L	L	L	H	H
	WH	9	H	H	L	L	L	L
	UL	12	H	L	L	L	L	H
	VL	11	L	H	H	L	L	L
	WL	10	L	L	L	H	H	L

c. Motor driver circuit section

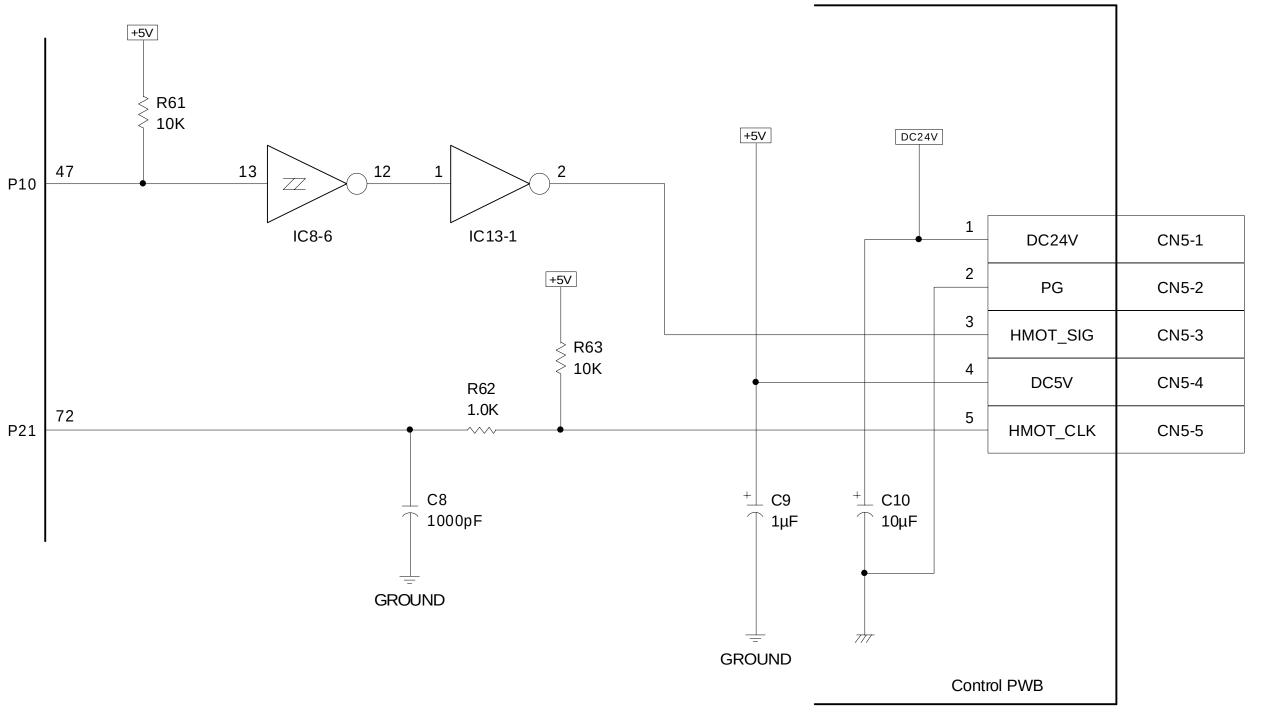
Q1 ~ 6 form the bridge circuit to supply power to the motor coils (U, V, W phase). Q7 ~ 9 are pre-drivers of Q4 ~ Q6. The ON/OFF timing of Q1 ~ Q6 is the output section of the logic diagram of IC1 in b. (refer to above diagram) ON when HIGH. I3 1 ~ 3 pins control the motor speed by turning ON/OFF Q4 ~ Q6 with output signals (uH) from the IC1 and PWM signals outputted from the CPU.

d. Pulse signal (PLS) generating circuit

When the magnet passes the PWB pattern just below the rotor, an induced voltage of sine waveform is generated across the pattern. This is a minute voltage sine waveform, and is amplified by IC2.2 and formed by IC2.1 into the pulse waveform.

e. PWM signal generating circuit

The CPU compares the PLS signal with the reference CLK generated in the CPU to generate the PWM signal. When the speed of the PLS signal is greater than the reference CLK, it is judged that the motor is rotating at a higher speed than the specified speed. In that case, the PWM signal duty ratio is decreased to decrease the speed. When the PLS signal is slower than the reference CLK, is judged that the motor is rotating slower than the specified speed. In that case, the PWM signal duty ratio is increased to increase the motor speed.

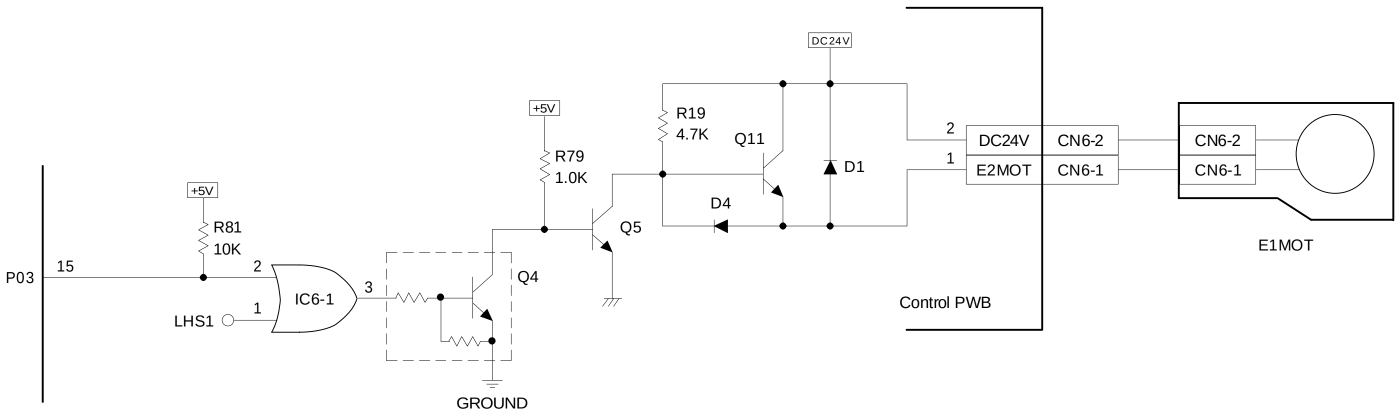


HMOT drive circuit

B. Lift motor drive circuit (E1MOT, E2MOT)

The lift up motor is rotated to lift the paper in the paper tray 3 to the transport level. The lift motor drive circuit drives the lift motor. There are two sets of the lift up mechanism, each one is provided with the motors (E1MOT, E2MOT) and the drive circuit. These two are of the same composition. In the following description, the E1MOT is described.

The lift motor is turned on/off by the CPU. When the level sensor 1 (LS1) described in the sensor section is turned off during paper transport, the CPU turns on the lift motor (E1MOT) to turn on the sensor. The ON signal is outputted from the IC1-15 pin. The logical sum of this signal and the limit sensor 1 (LMS1, HIGH when limited) is taken. Only when the limit sensor 1 is OFF (LOW), it is outputted from the IC6-3 pin. When the IC6-3 pin becomes LOW, a current is not supplied to the Q4 base, and Q4 is turned off. As a result, a current is supplied to the Q5 base from R79 to turn on Q5 and to drive CN6.1 pin to about 0V. A voltage difference is generated between the both poles of the motor to supply a current to the motor. When the level sensor detects the paper surface, the IC1-15 pin becomes HIGH to turn off Q5. At that moment, a voltage difference is generated between the base and the emitter of Q11 to turn on Q11 and apply brake. D1 is the flywheel diode which operates at OFF.

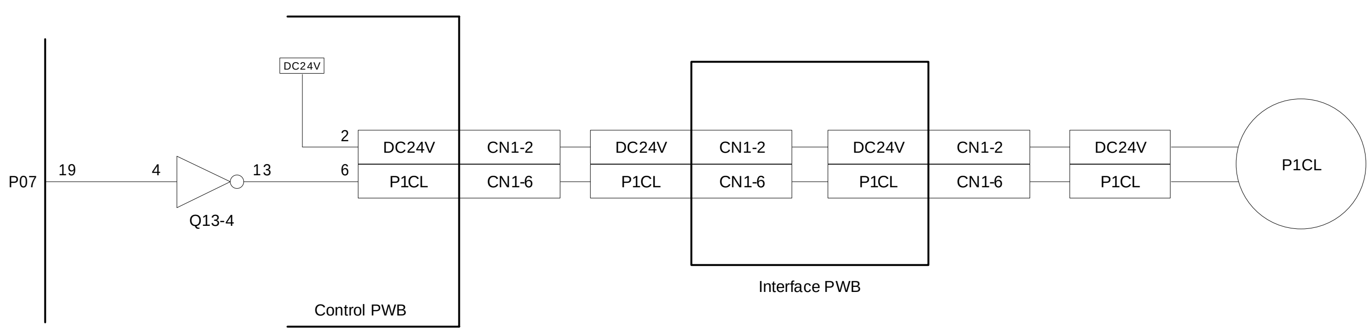


E1MOT drive circuit

C. Pickup clutch (P1CL, P2CL), separation clutch (BCL), resist clutch (RCL) drive circuit

The clutch transmits the paper transport motor (HMOT) drive power to the rollers, and it is of the same composition as the pickup clutches (P1CL, P2CL), the separation clutch (BCL), and the resist clutch (RCL). In the following description, the pickup clutch 1 ((P1CL) is described.

Q13 (TD62003) is the Darlington driver with seven circuits, one of which is used to drive. When the IC1-19pin becomes HIGH, the transistor at the output stage of Q13.4 is turned on to drive IC13-13 pin to about 0V, supplying the power to the clutch and transmitting the power.



P1CL drive circuit

D. Other circuits

(a) Reset circuit

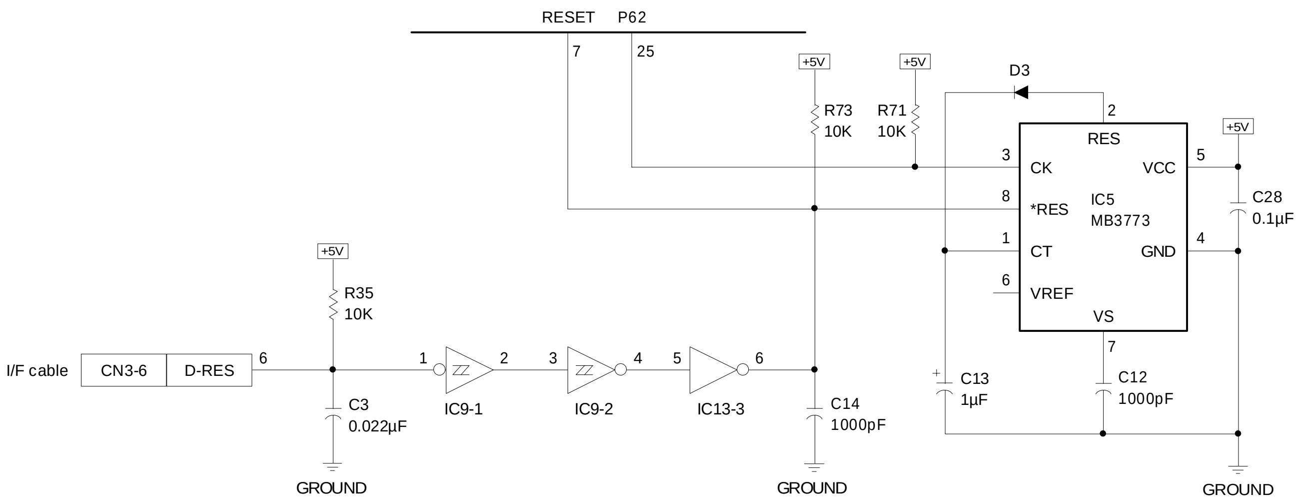
The reset signal generates the CPU reset signal, and is composed of the IC5 and the peripheral circuits. The IC5 has the integrated reset functions of the power ON reset, the CPU reset in case of abnormally low voltage of +5V, and the watch-dog timer function.

When the power is supplied and the power line (+5V) reaches about 0.8V, the IC5 start operation. The IC5-8 pin becomes LOW to rest the CPU. When the power line reaches about 4.3V, the reset state is retained for the time (about 100ms) determined by the capacity of C13. After passing the retaining time, the IC5-8 pin becomes HIGH to cancel the reset, and the CPU start operation.

When the power line falls to about 4.2V, the IC5-8 pin becomes LOW similarly to reset the CPU. This state is canceled after 100ms from the moment when the power line reaches 4.3V.

The IC5-3 pin is the watch-dog timer clock input pin, and receives the regular pulse signals of 10ms frequency outputted when the CPU is normally operating. If this signal is stopped because of hung up of the CPU, etc., the IC5-8 pin is driven LOW in a certain time to reset the CPU. The clock monitoring time is also determined by the C13 capacity (about 100ms).

Hard reset is also available from the PPC body through the communication cable. In this case, CN3.6 pin is driven HIGH or opened to reset. The IC9.1, 2 are for logical sum. The IC13.3 is the open collector element to compose the IC5 reset output and the hard reset.



Reset circuit